

# bittide: Control Time, Not Flows

First Time Hardware Implementation and Validation

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Hot Interconnects, 2025

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**QBayLogic.**

**Google**

**Stanford  
University**

# This talk

- Introduction to bittide
- What hardware we built
- What we measured

# Introduction

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Clock cycle accurate synchronization at datacenter scales

Ahead of time scheduling

# Promises

Ahead of time scheduling

Zero in-band overhead

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Zero in-band overhead

Decentralized

# Promises

Ahead of time scheduling

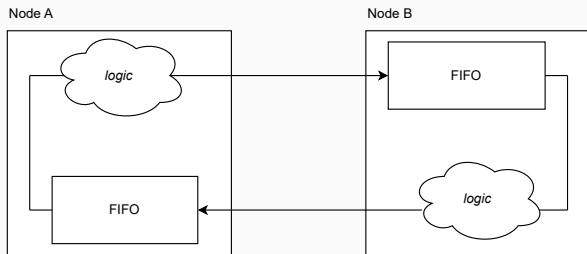
Zero in-band overhead

Decentralized

Simple

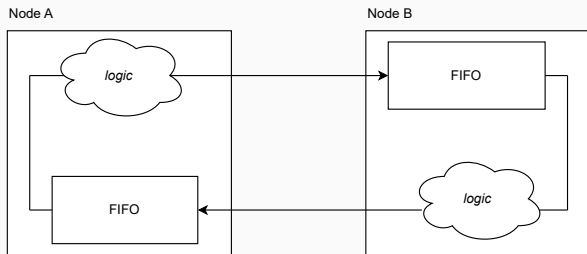


# How



FIFO on each incoming link

# How



FIFO on each incoming link

Must not under or overflow

Start with FIFOs half-full

Start with FIFOs half-full

**Speed up** when buffers fill

Start with FIFOs half-full

**Speed up** when buffers fill

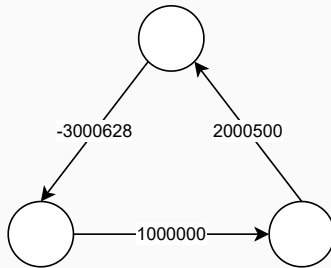
**Slow down** when buffers drain

# Clock control

Start with FIFOs half-full

**Speed up** when buffers fill

**Slow down** when buffers drain



RTT: 128

# Implementation

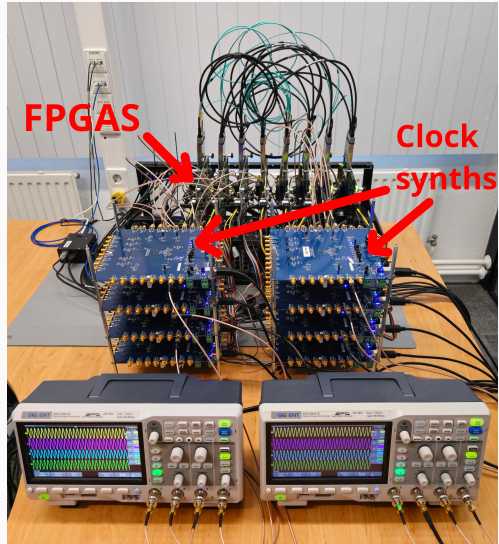
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# System architecture

8 fully connected FPGAs

8 clock synthesizers

External measuring equipment

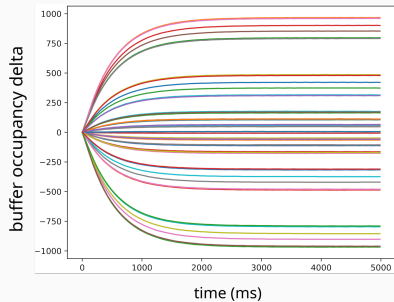




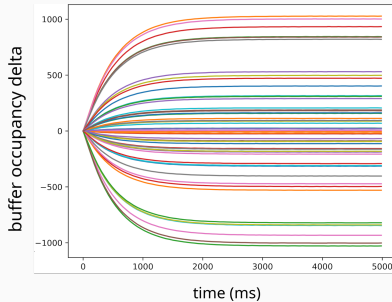
# Measurements and validation

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# Fully connected

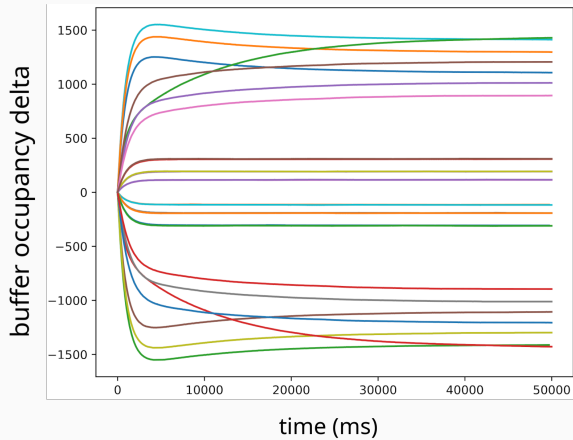
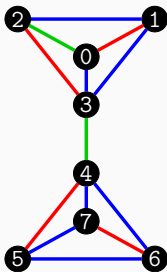


2m



2km

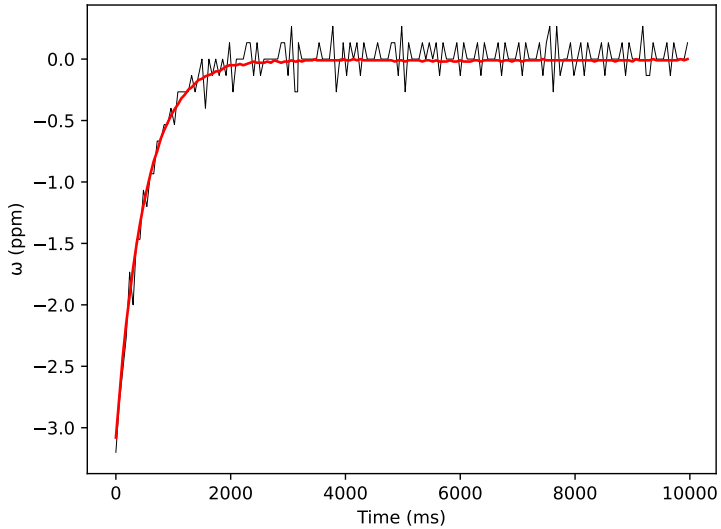
# Hourglass



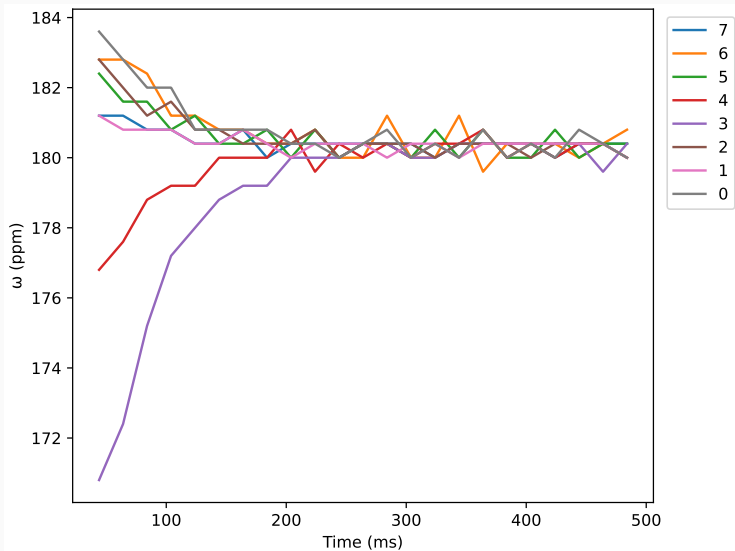
## RTTs in clock cycles

| FPGA | 1           | 2  | 3  | 4  | 5  | 6  | 7  | 8 |
|------|-------------|----|----|----|----|----|----|---|
| 1    |             |    |    |    |    |    |    |   |
| 2    | 68          |    |    |    |    |    |    |   |
| 3    | <b>1299</b> | 68 |    |    |    |    |    |   |
| 4    | 67          | 68 | 68 |    |    |    |    |   |
| 5    | 68          | 68 | 68 | 70 |    |    |    |   |
| 6    | 69          | 67 | 68 | 69 | 69 |    |    |   |
| 7    | 69          | 70 | 69 | 68 | 69 | 68 |    |   |
| 8    | 69          | 69 | 69 | 70 | 69 | 70 | 68 |   |

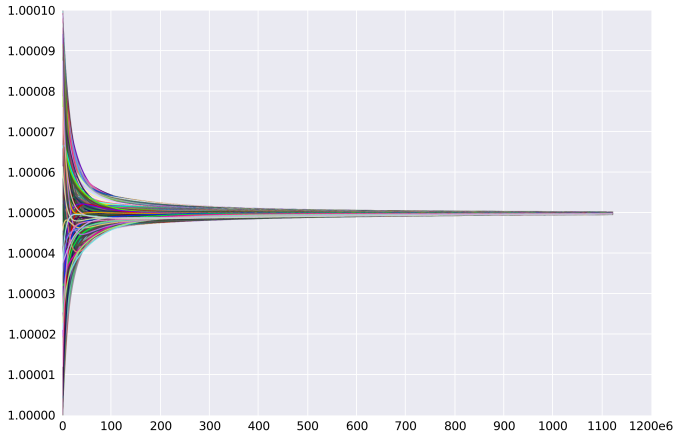
## Comparison against model



# Aggressive gain



# Scalability



## Conclusion

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# Summary and contributions

bittide synchronization scheme:

- ahead of time clock cycle scheduling
- zero in-band overhead
- decentralized
- simple

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bittide synchronization scheme:

- ahead of time clock cycle scheduling
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- decentralized
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First hardware implementation

- only off the shelf components
- model very closely matches measurements
- clock control incredibly stable

## Open source resources

- **Project website:** [www.bittide.io](http://www.bittide.io)
- **Hardware repository:** [github.com/bittide/bittide-hardware](https://github.com/bittide/bittide-hardware)
- **Clock control simulation:** [github.com/bittide/Callisto.jl](https://github.com/bittide/Callisto.jl)

# Questions?