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Transforming connectivity with ultra-fast µLEDs

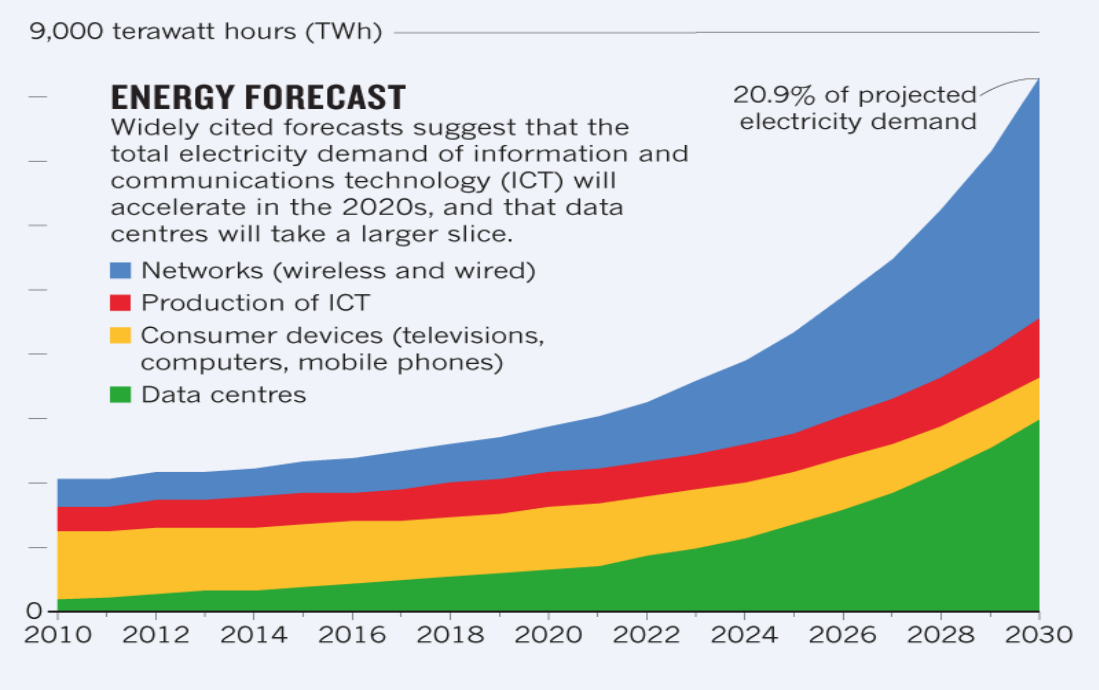
Paradigm Shift in AI Clusters using microLED based Interconnects

Chris Pfistner

Hot Interconnects 2025

AI Networks – Energy Efficiency and Bandwidth Density Needs

IT projected at > 20% of world electricity by 2030



LLM outpacing memory bandwidth 100,000x

Using optimized interconnect technology is absolutely critical!

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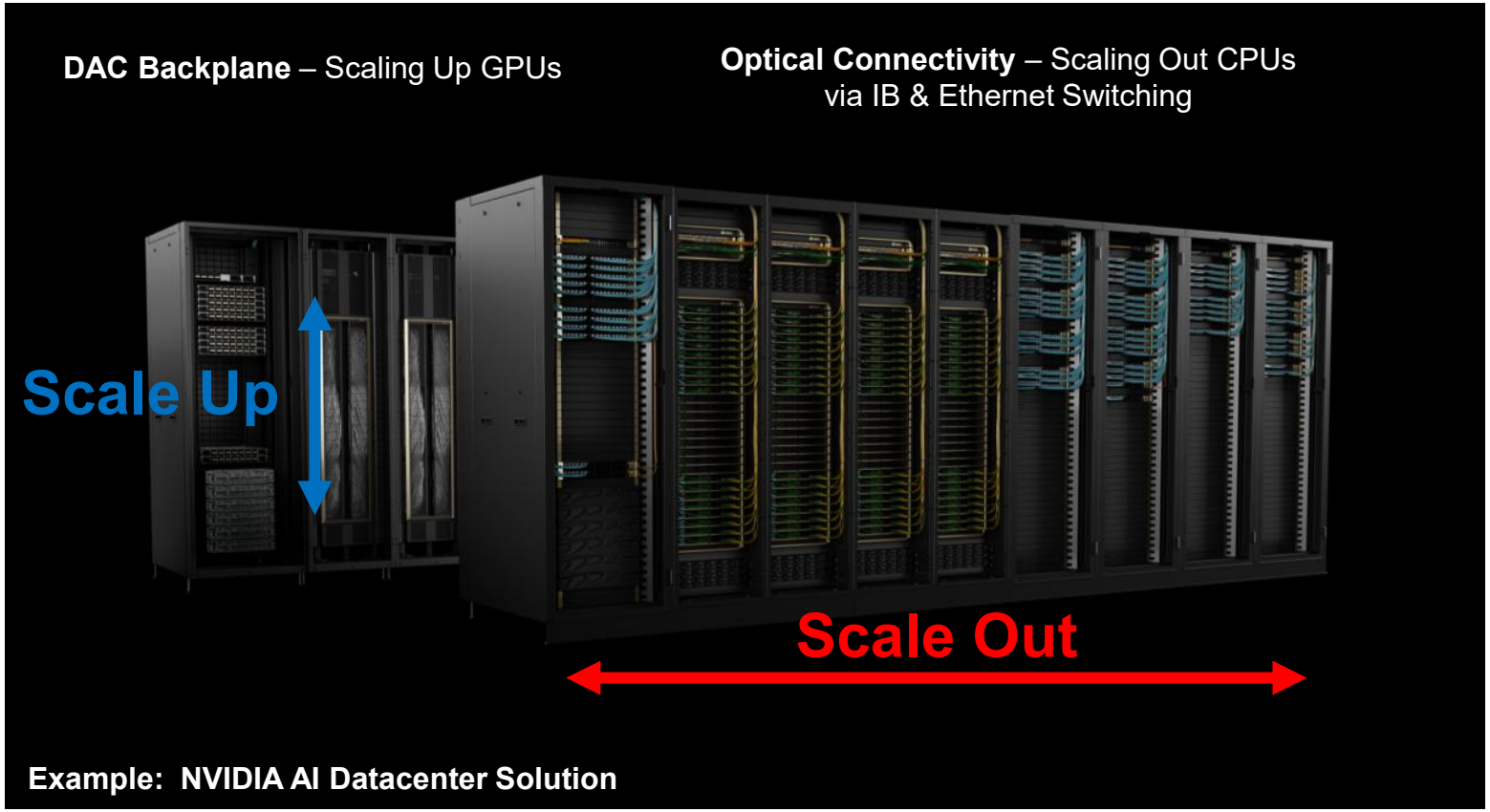
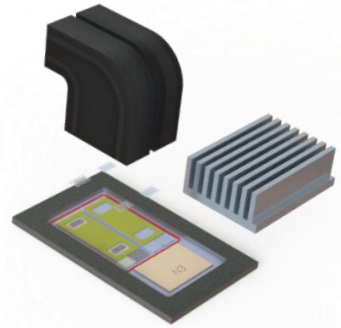
3 Network Segments in AI – Different Interconnect Technologies

- **Inter Datacenter:**
  - **Transport Networks**
- **Intra Datacenter:**
  - **Scale Out:**
    - TRV DSP, LRO, LPO
    - CPO
  - **Scale Up:**
    - Today: Copper
    - Tomorrow: ???



LightBundle Interconnect - Ideally Suited for Scale Up Networks

Exploded View:



Key Specs for Scale Up:

Parameter	Performance
Energy Efficiency *	<< 5pJ/bit
Shoreline Density	> 1Tbps/mm
Reach	10m
Reliability	10 FIT
Cost Target 2030	$0.10/Gbps

* Optical Link including Driver, Laser/LED, PD, TIA, LA

LightBundle:

< 1pJ/bit (NRZ format)

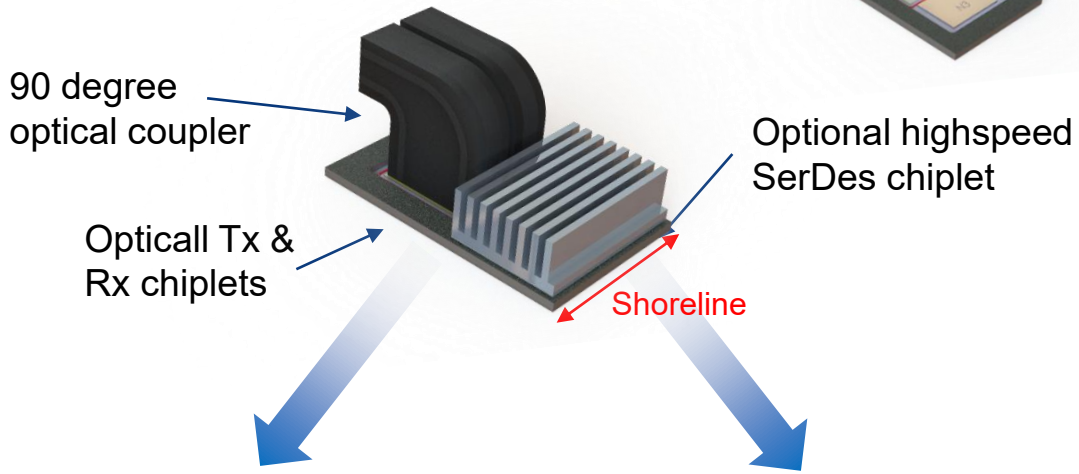
1Tbps/mm (2D array)

10m – 20m

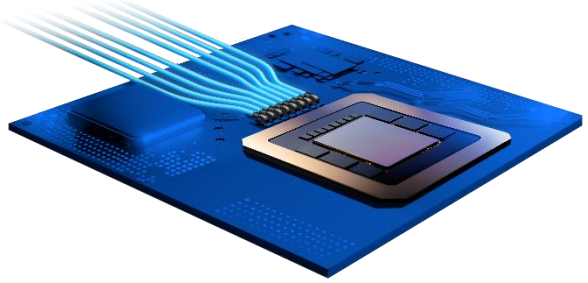
GaN LEDs:

- very reliable
- Op. Temperature:
  -55° to 125°C
- cost effective

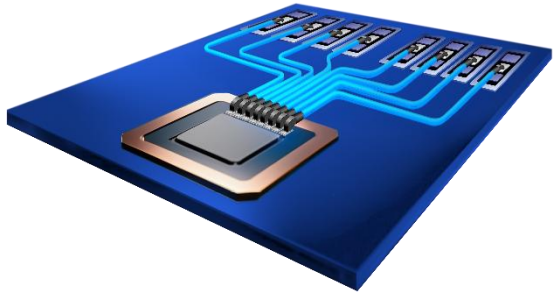
Modular Architecture:



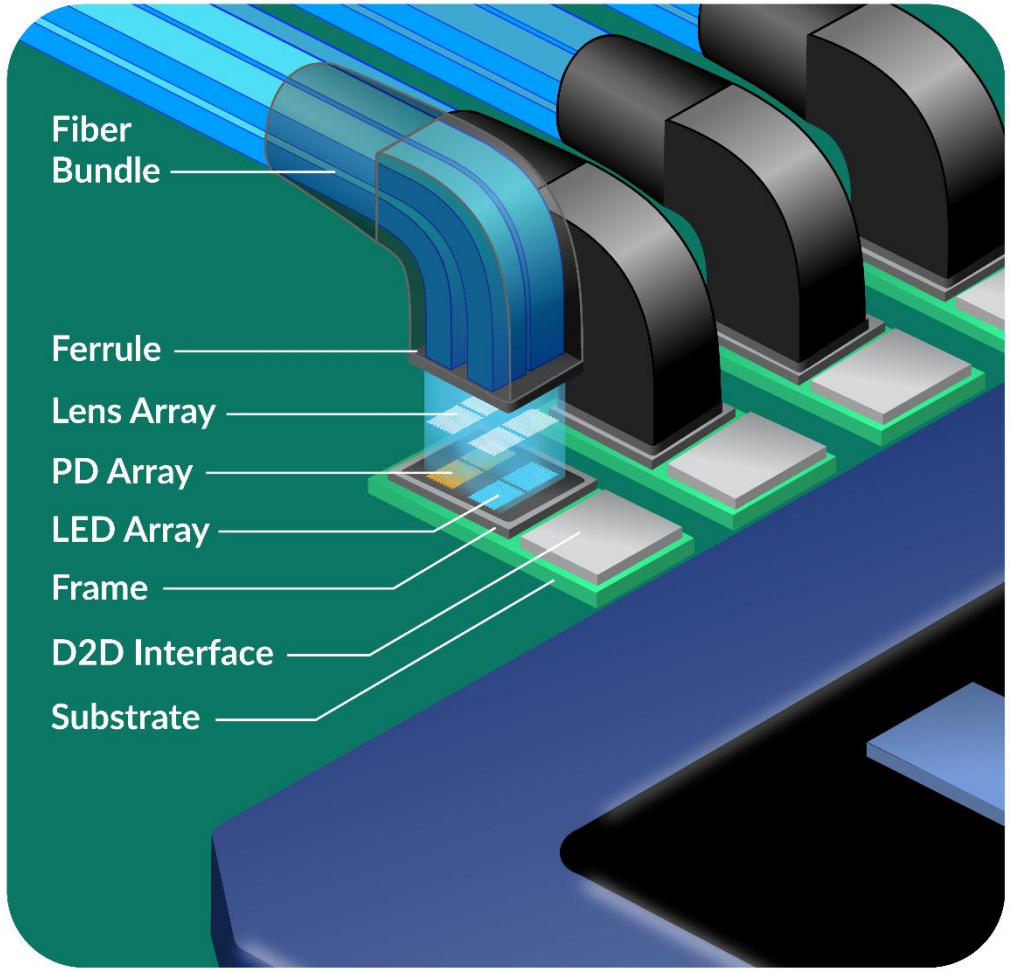
1.6Tbps OBO Module:

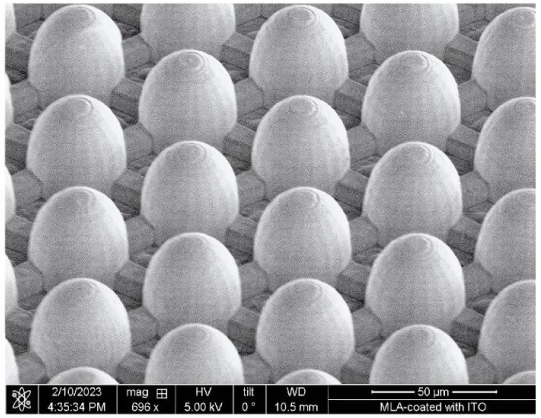


12.8Tbps CPO Module:

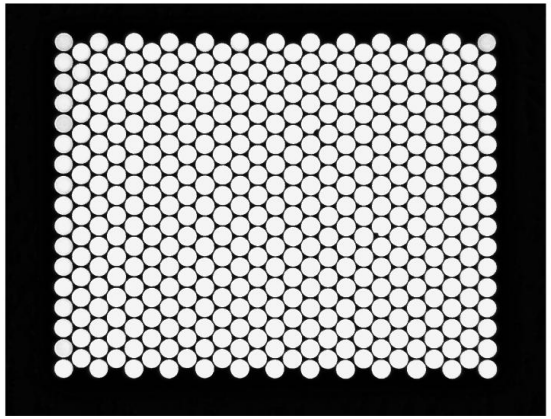


How does the Avicena LightBundle™ solution work

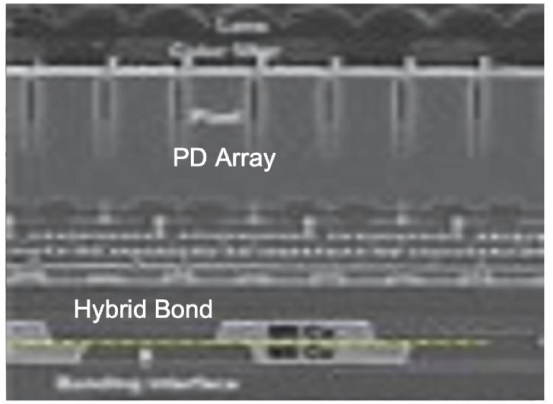




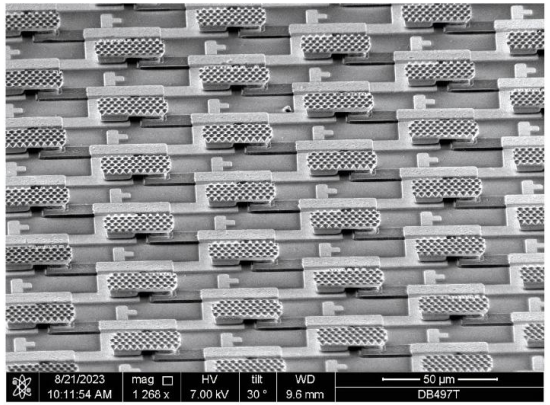
Lens Array



Fiber Bundle Cross Section

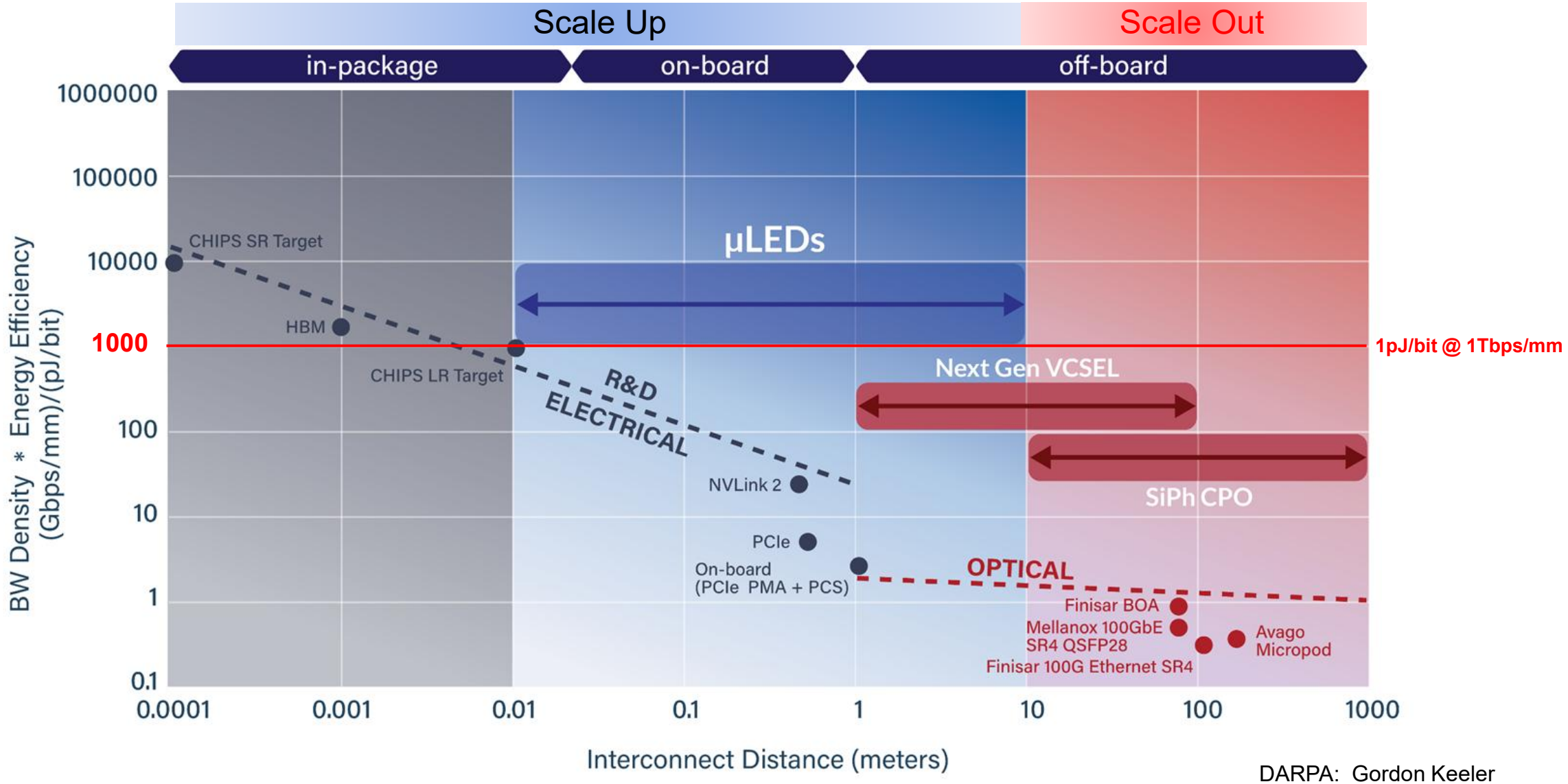


CIS PD Array



µLED Array

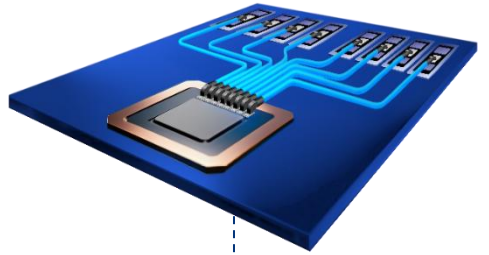
Beach Front Density & Energy Efficiency against Link Distance



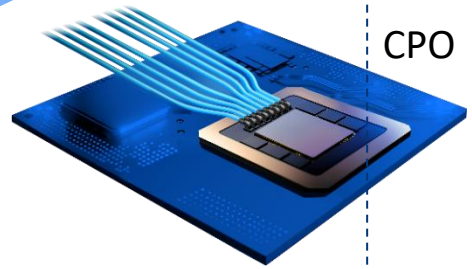
DARPA: Gordon Keeler

Avicena Top-Level Roadmap for Scale Up

Optical Memory Interconnects



CPO



6.4T to 12.8T
HD Pluggable Connector

1.6T AOC

4 x 224 G = 896 G
Demo Kit

2025 2026 2027 2028 2029 2030

Latest Technical Achievements

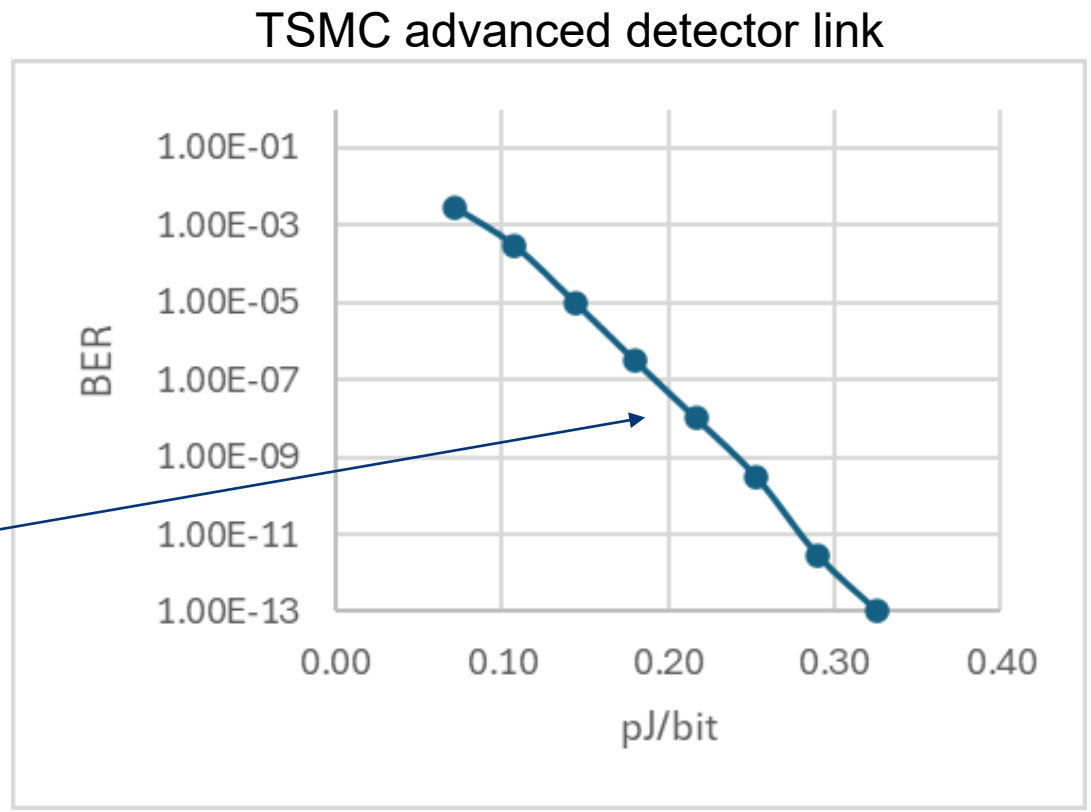
- Demonstrated 16G per lane performance

- Using TSMC made advanced detectors show ultra-low power single lane performance.

Tx energy efficiency is ~20x better than Silicon Photonics

4Gbps, P_in =3µW, I_LED= 250uA:

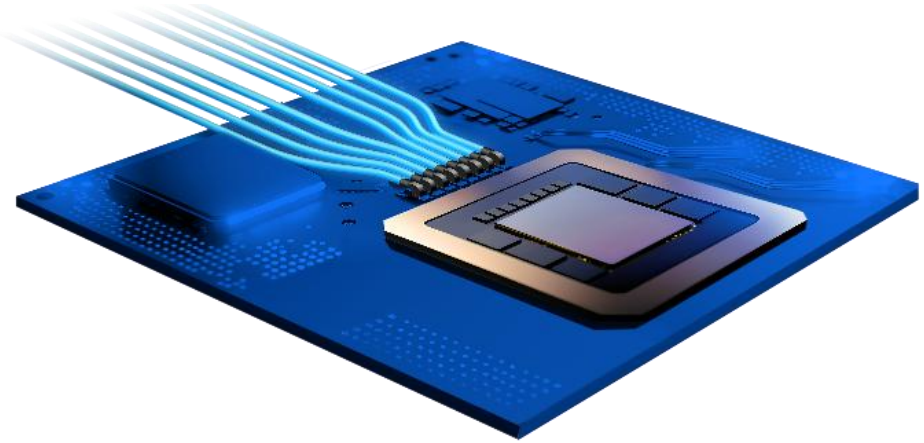
- BER ~3E-7 @ 0.20pJ/bit



Conclusion: µED Interconnects are ideally suited for Scale Up networks

Key Specifications:

Parameter	Performance	Comments
Energy Efficiency	< 1pJ/bit	Incl. Driver, LED, PD, TIA, LA Direct Modulation NRZ
Shoreline Density	> 1Tbps/mm	2D array future: >> 1Tbps/mm
Reach	10m – 20m	Up to 30m with lower energy efficiency
Operating temperature	-55° to 125°C	Demonstrated up to 400°C



Additional Notes:

- 16G per LED demonstrated in our labs – July 2025
- GaN LEDs are highly reliable (e.g. lighting industry)
- Compatible with any CMOS process node - no specialty foundry required
- Integrated Si PD very well suited for 425nm detection
- Multimode → relaxed assembly tolerances
- Cost effective

Thank You!

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