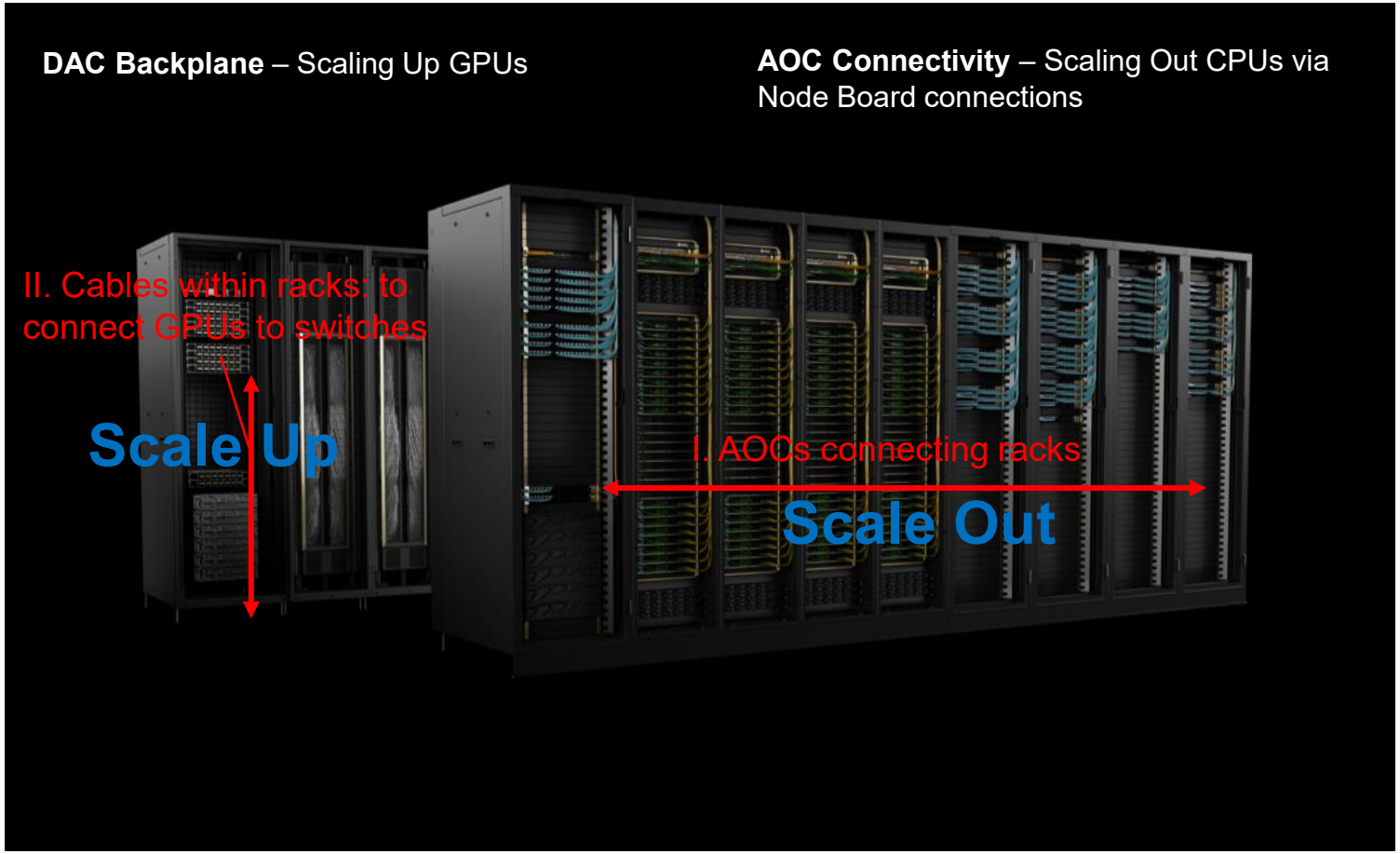
AVICENA

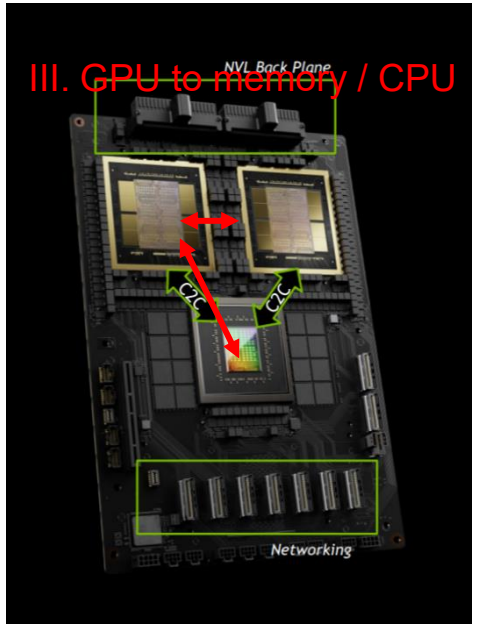
Transforming connectivity with ultra-fast µLEDs

Micro-LED data interconnects Applied Materials Workshop

August 22, 2025

3 length scales in AI clusters – which technology is best for each?





I. Addressed with standard laser-based optics, moving to CPO
II. Copper cables now, but for scaling, reach is critical
III. Copper traces, Impending

II, III have fundamentally different requirements than traditional fiber optics

Scale up (II) opportunity is now and is huge

Key Specs for Scale Up:

Parameter	Performance
Energy Efficiency	<< 5pJ/bit
Shoreline Density	> 1Tbps/mm
Reach	10m
Reliability	10 FIT
Target Cost	$0.10/Gbps

- At 4 million GPUs/yr,
- 16Tb/s per GPU and
- 10¢/Gbps

➔ $6B market for scale-up

➔ Need a different kind of optics: cost, reliability, energy efficiency are critical and can't be met with standard optics

Using telecom technology for chip-to-chip is challenging

At Kaiam in 2017 we did a 1.6Tb/s copackaging demo, and it was hard!! Many of the problems we encountered still remain

- Tight packaging tolerances
- Complex (Isolators, AR coatings, *stabilizing rings, λs*…)
- Poor laser reliability (high temp). ELS is expensive and complex
- Specialized detectors (Ge or InGaAs,..)
- High power consumption (lasers, modulator losses), high heat load
- Yield / cost issues

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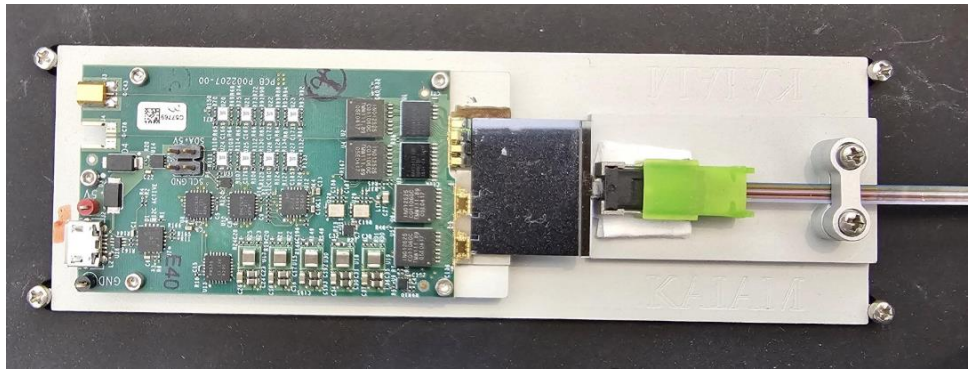
Kaiam and Corning Demonstrate Co-Packaged Photonic Interconnect (CoPPhI) for Terabit Chip Interconnect at OFC 2017

Potential to Reduce Chip Power Consumption by Half

March 21, 2017 10:51 PM Eastern Daylight Time

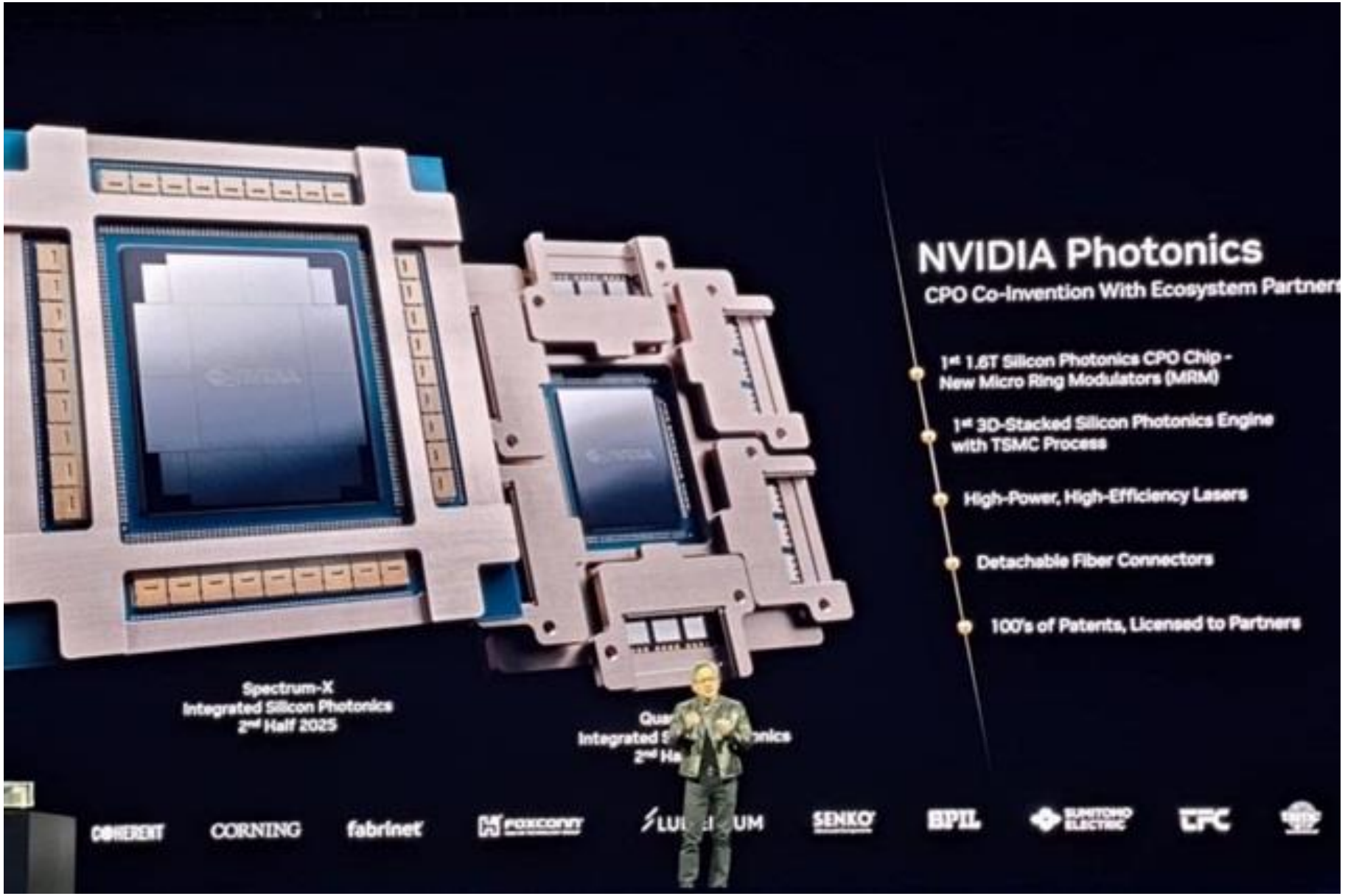
LOS ANGELES--(BUSINESS WIRE)--Kaiam Corp. and Corning Incorporated (NYSE:GLW) are showcasing an optical engine and single-mode fiber interface connector suitable for co-packaging with a 12.8 Tb/s switch chip at the 2017 Optical Fiber Communications Conference & Exhibition in the Los Angeles Convention Center this week. By converting high-speed signals to optical within the switch package, this high-density engine has the potential to cut chip interconnect power consumption in half.



"1.6Tb/s" module demo in 2017

(4 SM fibers each way, 4 wavelengths, 25Gb/s to 100Gb/s per wavelength)

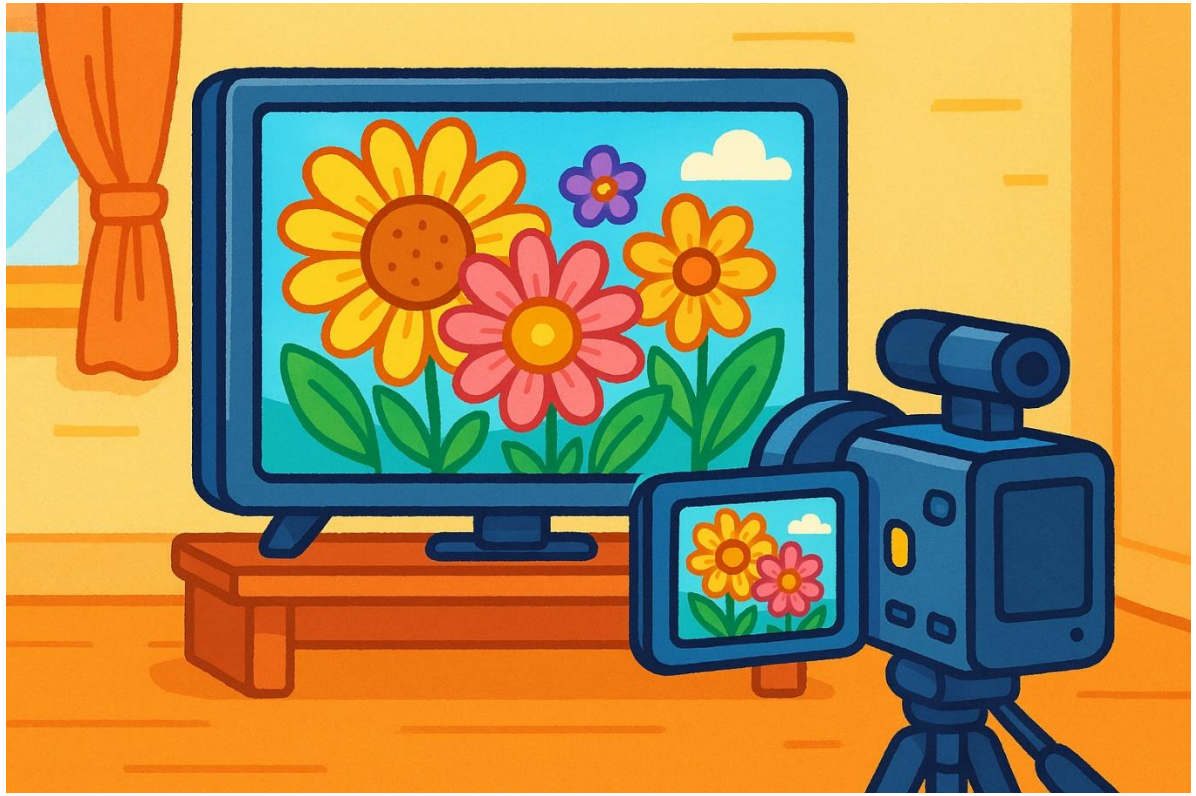
Nvidia announces CPO for scale-out in AI links



But acknowledges not good enough for Scale Up

Can we leverage another technology for this?

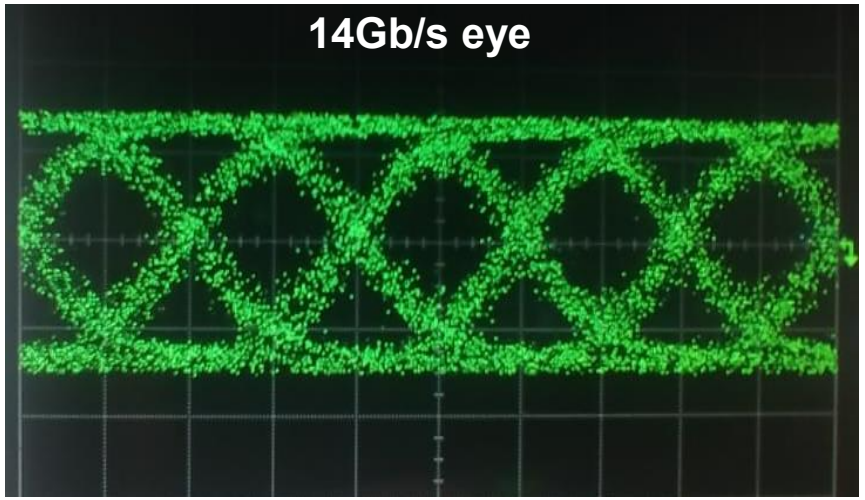
- Ideally wide bus and clock speed of chips (more like HBM bus)
- Ideally in big volume manufacturing already – cost reduced through scale
- High yield, highly reliable, very cheap.



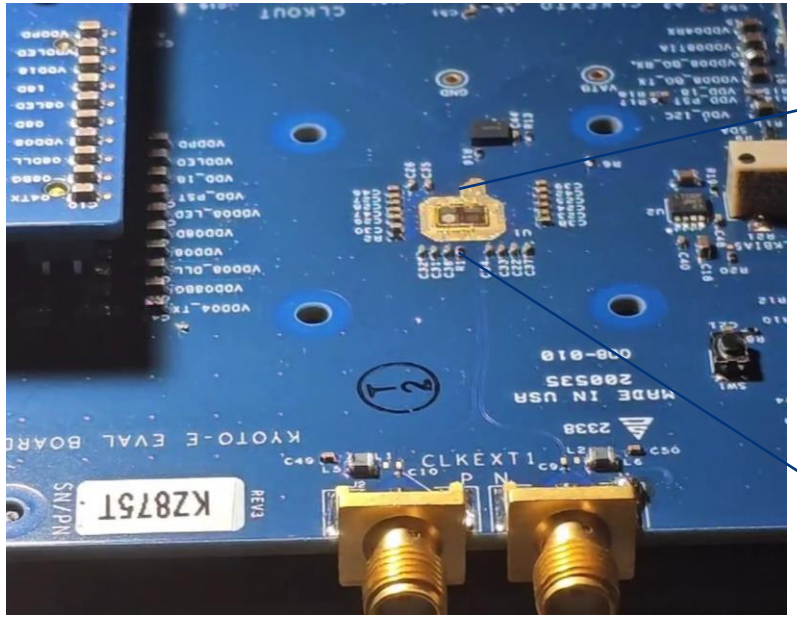
TV sending 2 million pixels at 60 frames a second, and camera receiving that data

Welcome a new magical device – high speed GaN microLED

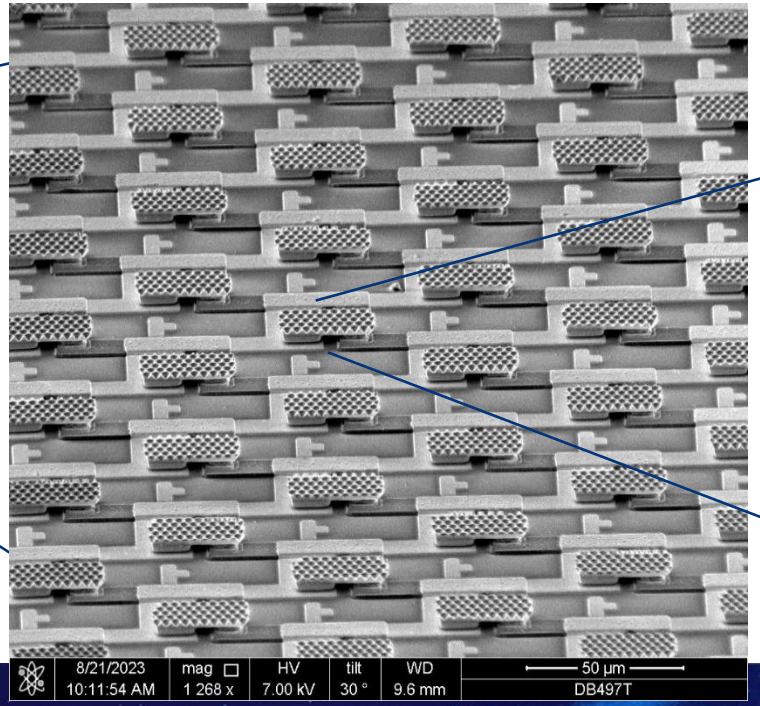
- Derivative of display device (millions on Si)
- Can modulate >10Gb/s per device
- NOT A LASER!
  - No threshold, no isolator, no polarization, no modes, no BER floors, no PAM4, high temp, reliable, low cost, massive parallelism (no SerDes)

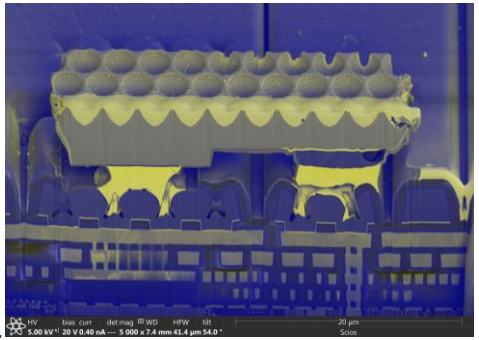


Million OLEDs/microLEDs arrays are used for displays, car headlights, and other applications



Arrays on silicon give optical output





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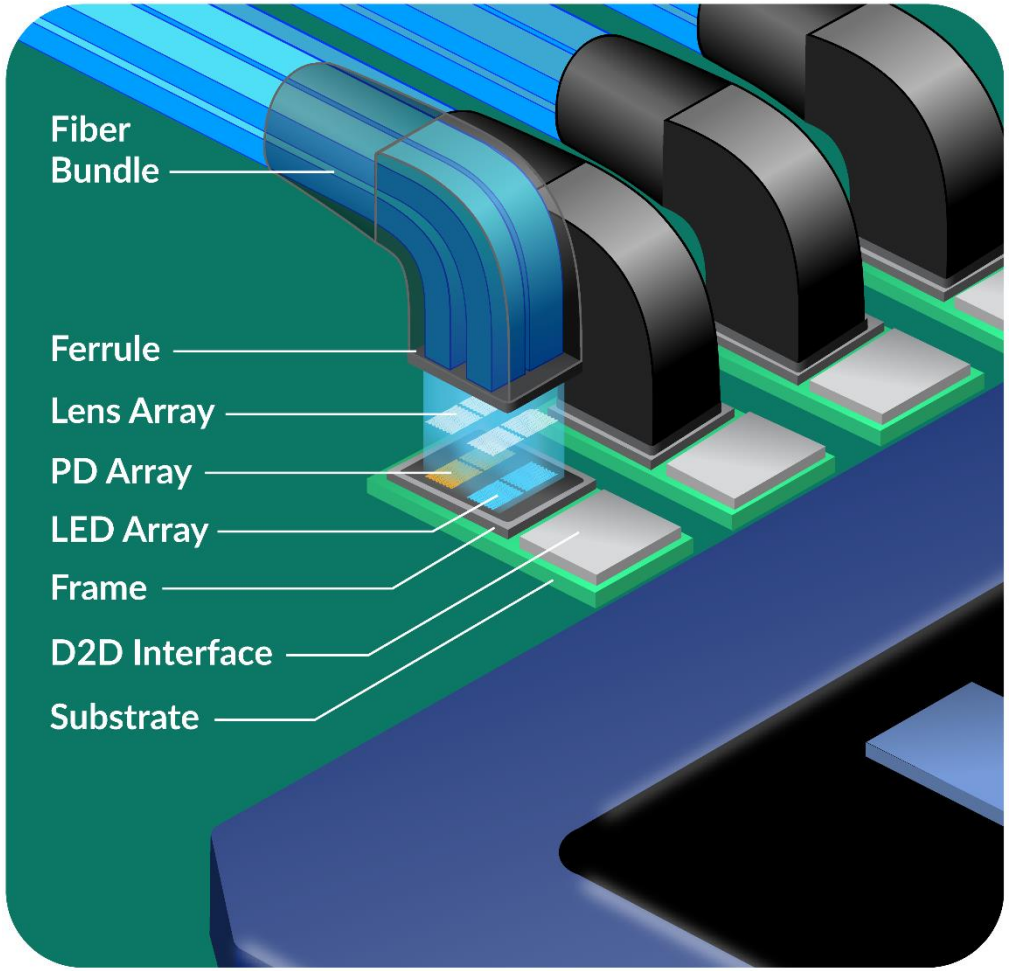
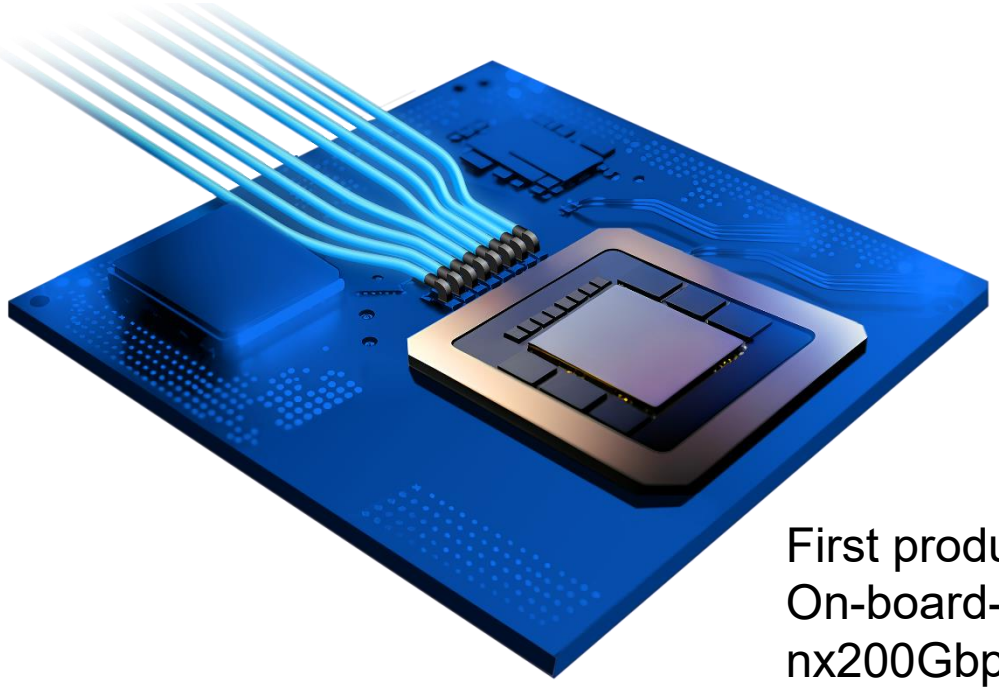
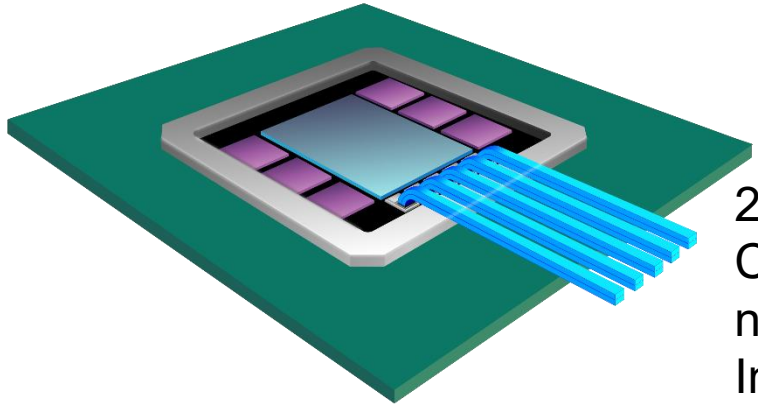
Product: From On-Board-Optics to Copackaged





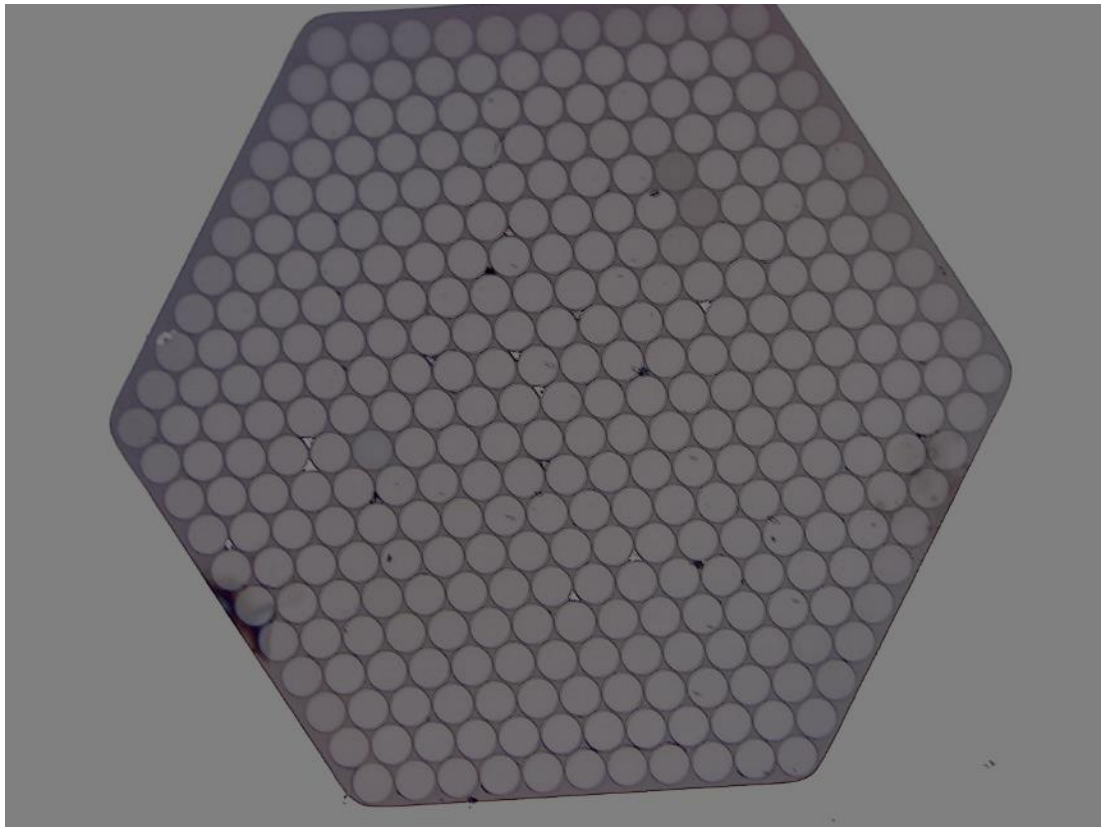
First product
On-board-optics,
nx200Gbps interface



2nd product
CPO,
nx32Gbps UCIe
Interface

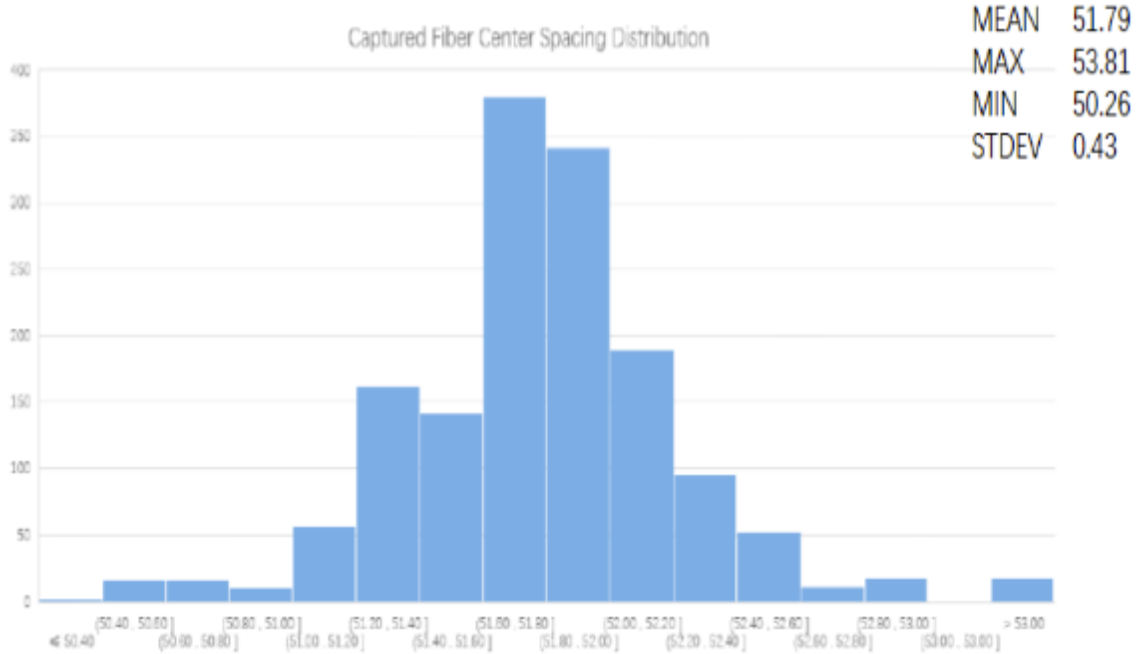
Cable of Lighting Fiber Arrays

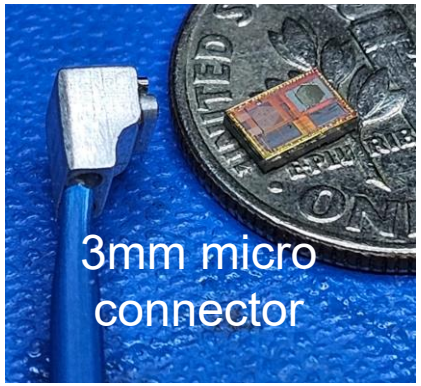
Fabricated arrays of lighting fibers. One beam per fiber



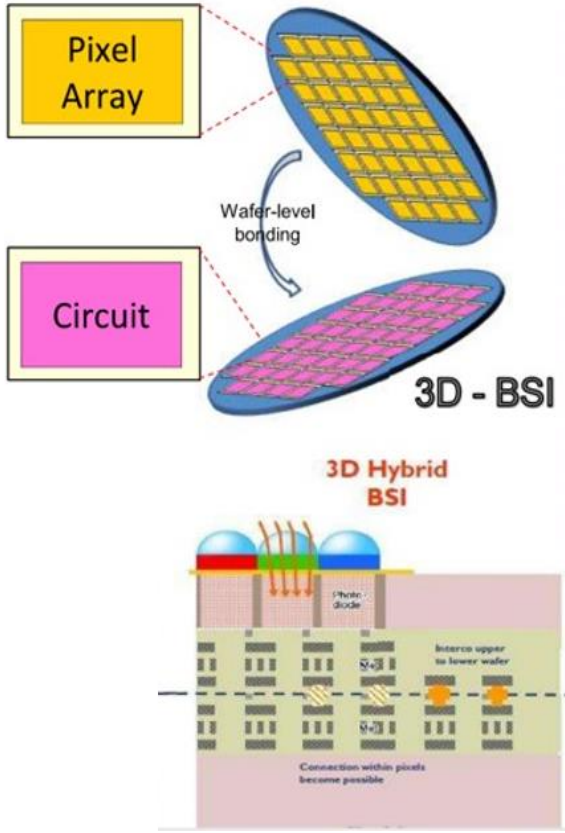
Array of 331 x 50um diameter illumination fibers

All fibers in the correct position

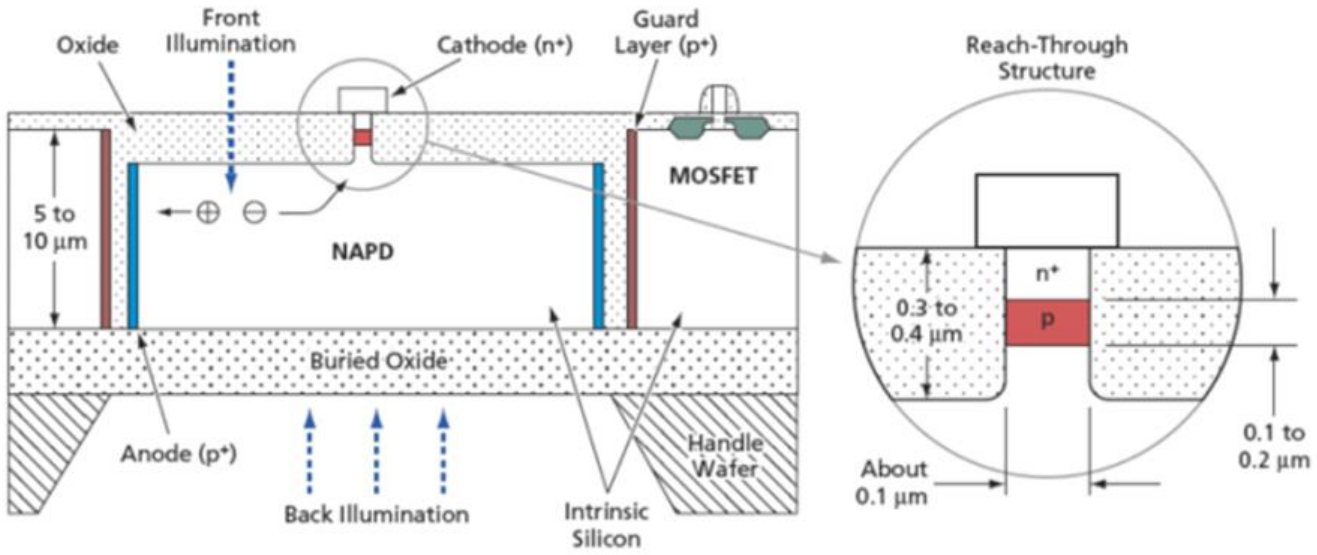




Leverage Camera technology



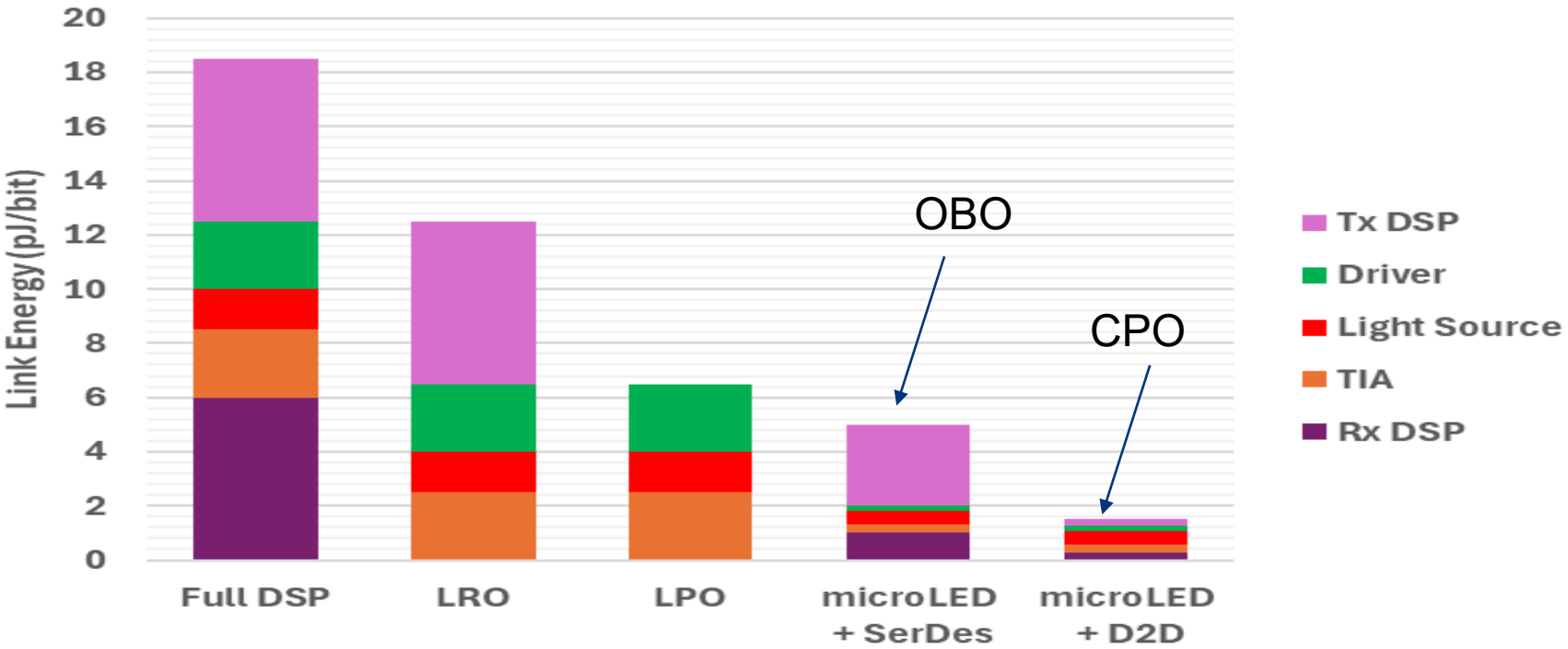
CIS process for PDs on CMOS w hybrid bonding



APD/SPAD for extreme sensitivity

- Can leverage CMOS Imager process – millions of pixels on CMOS
- SPADs / APDs give you 10dB-15dB more link margin
- TMSC press-release – tweaked camera process for us.

LightBundle is much lower power than standard solutions



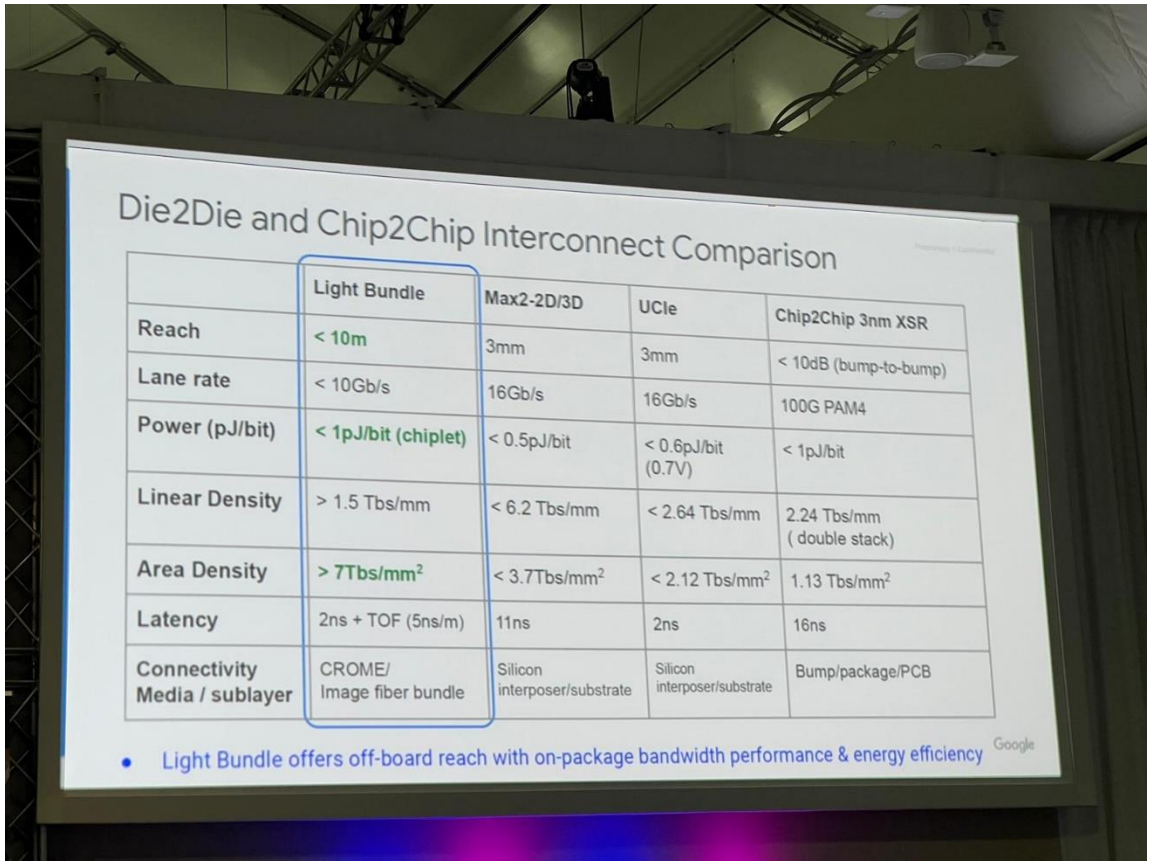
Notes:

- Low power “slow & wide” approach of microLED interconnects reduces optical power but still requires SerDes in current PAM4 eco-system
- Upcoming parallel interfaces such us UCIe will fully enable low power interconnects based on microLEDs

Pros / Cons

- Very simple packaging
- High temp, high yield, truly silicon compatible
  - Any node. Simple PDs
- 1pJ/bit - Pennies per Gbps
- High parallelism natural match to processors and memory
- Infrastructure already exists for high volume and low cost

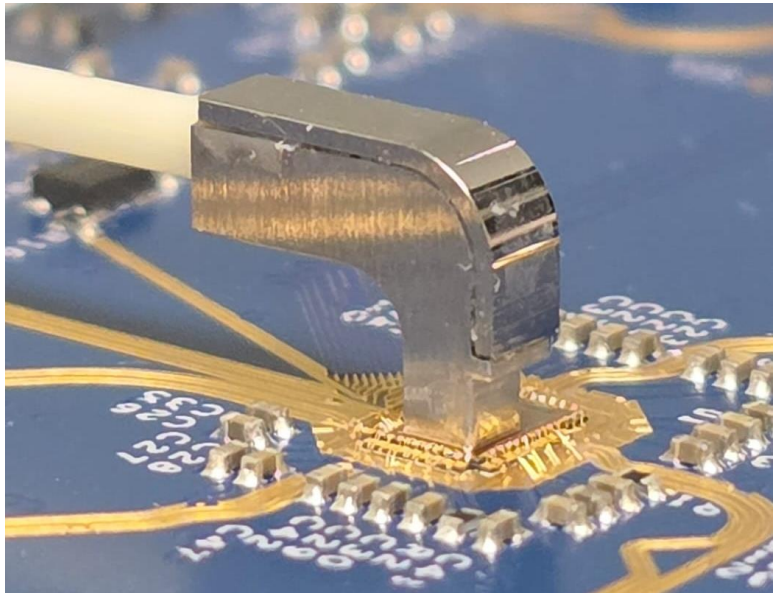
- BUT can’t do 100’s of meters

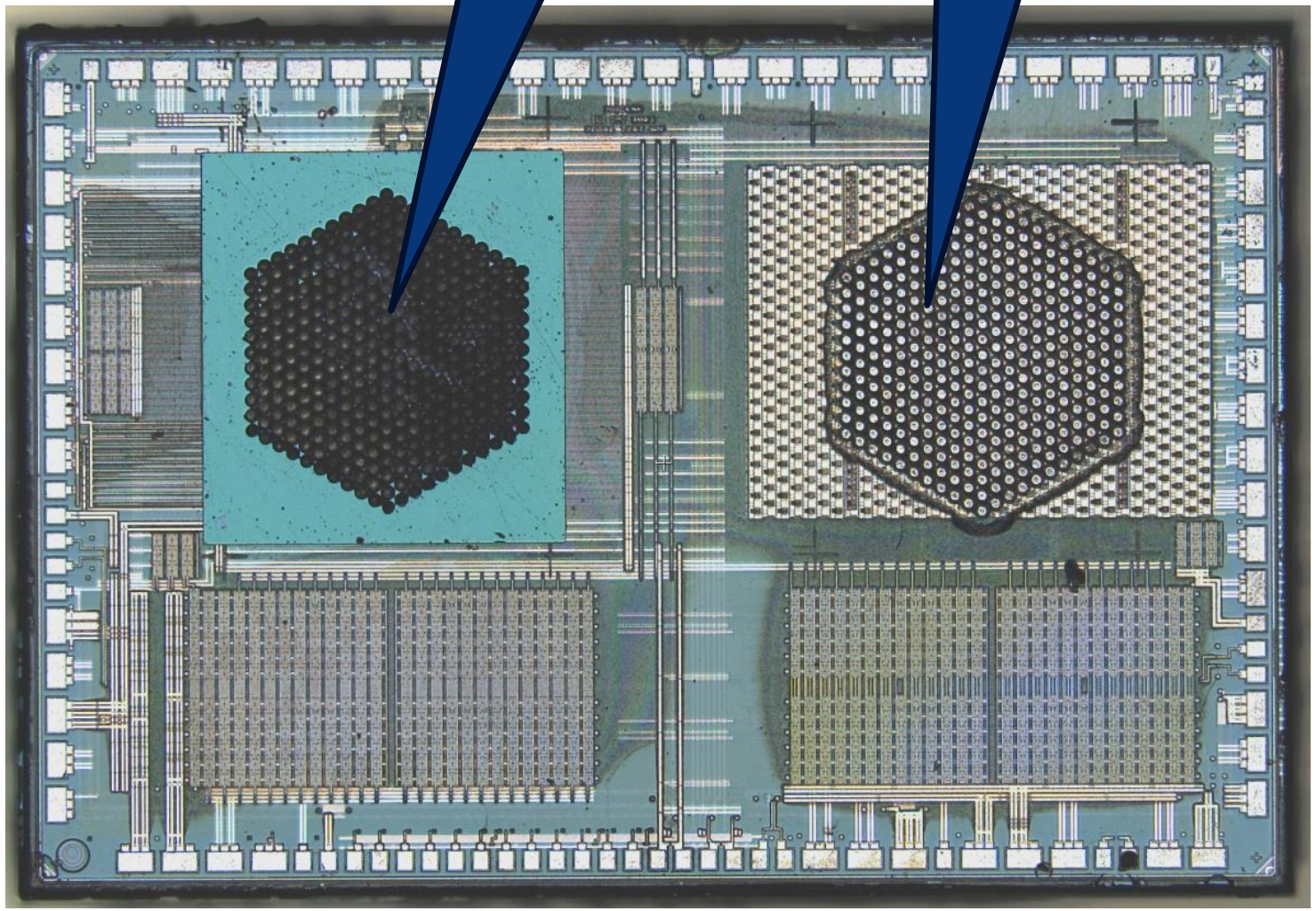


“Off-board reach with on-package bandwidth performance and energy efficiency”

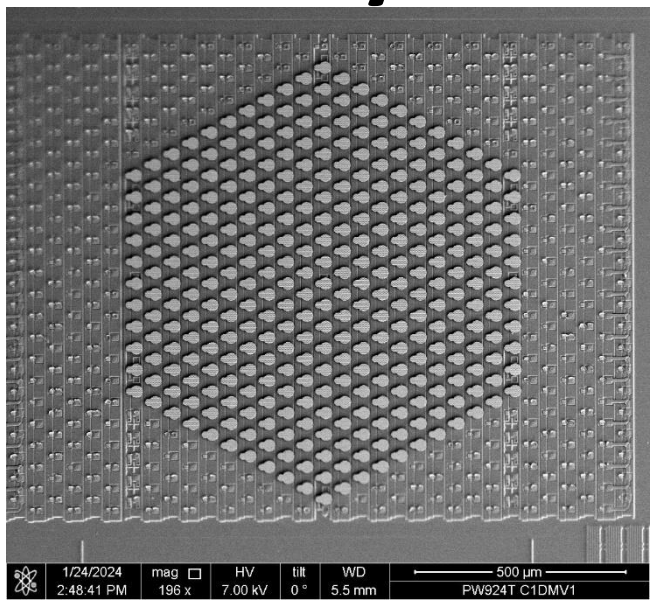
1Tb/s Demo chip

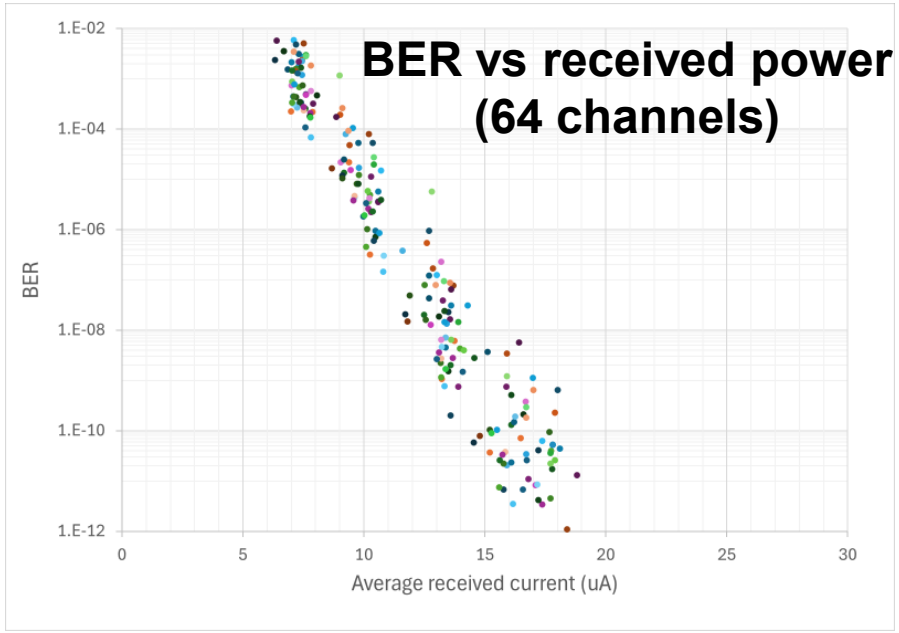
- TSMC N16 process
- 304 LEDs on 50µm grid
- 304 PDs on 50µm grid
- ~ 1.2Tbps (4Gbps/channel x 304 channels)
- link power < 1pJ/bit

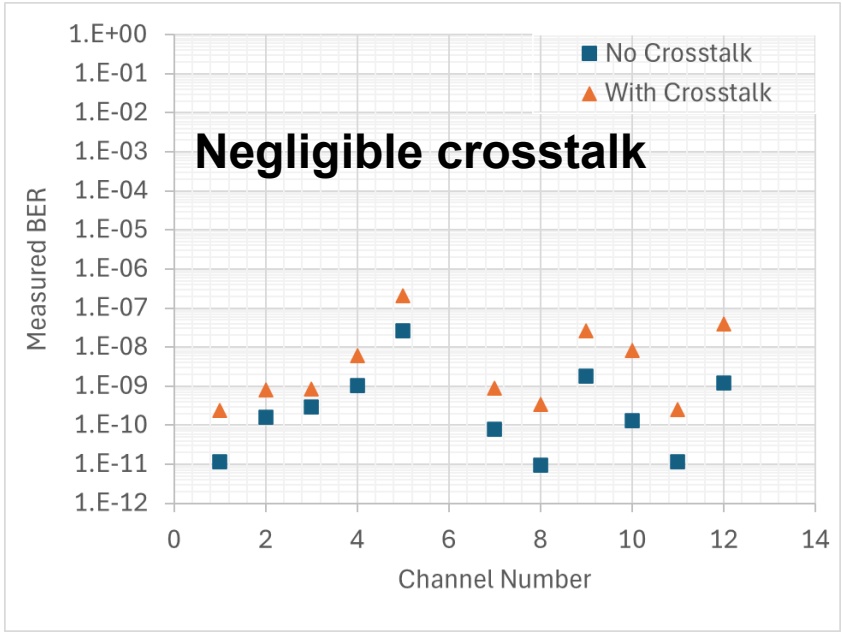




Tx arrays

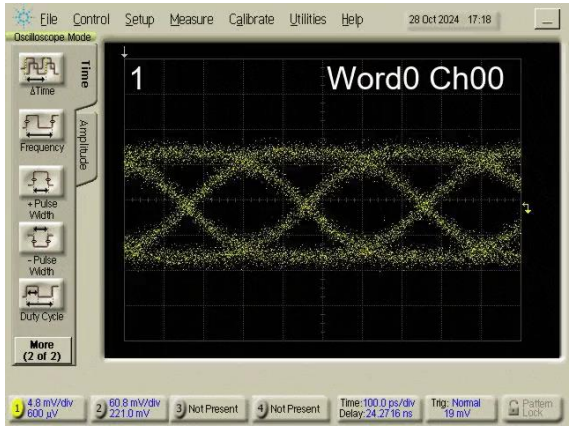






Yield notes

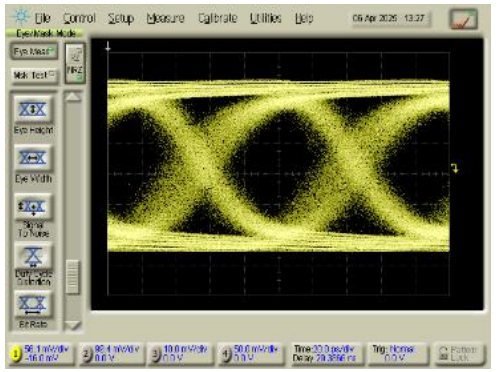
- Microlenses added to improve fiber coupling
- Nearly all arrays have 100% LED yield (display yields are >99.99%)
- Can also have redundancy (similar to parallel electrical links) so very tolerant of some bad LEDs



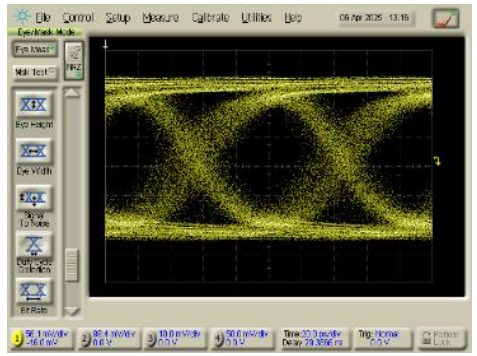
transmit eye @ 3.3Gbps

11.2Gb/s Single channel Tx

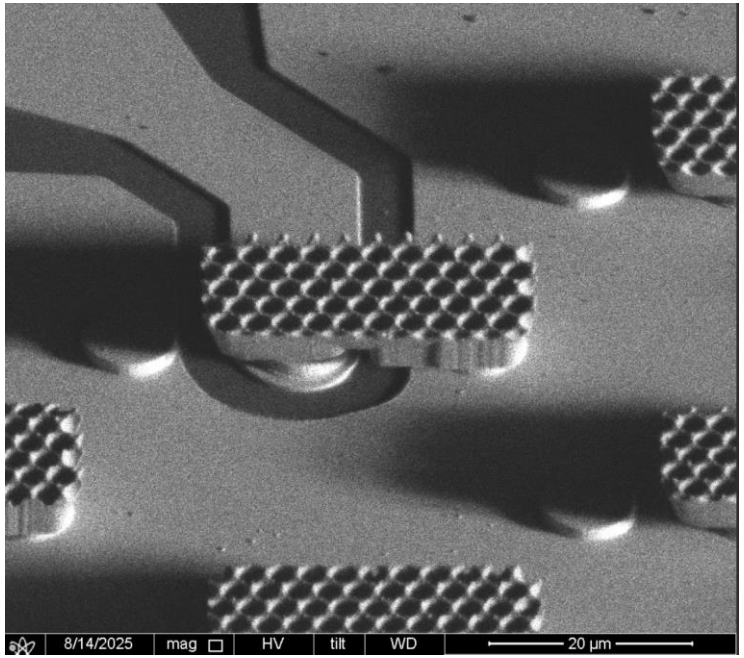
- Used reference transceiver
- Proper drive
- Hitting ~pJ/bit numbers

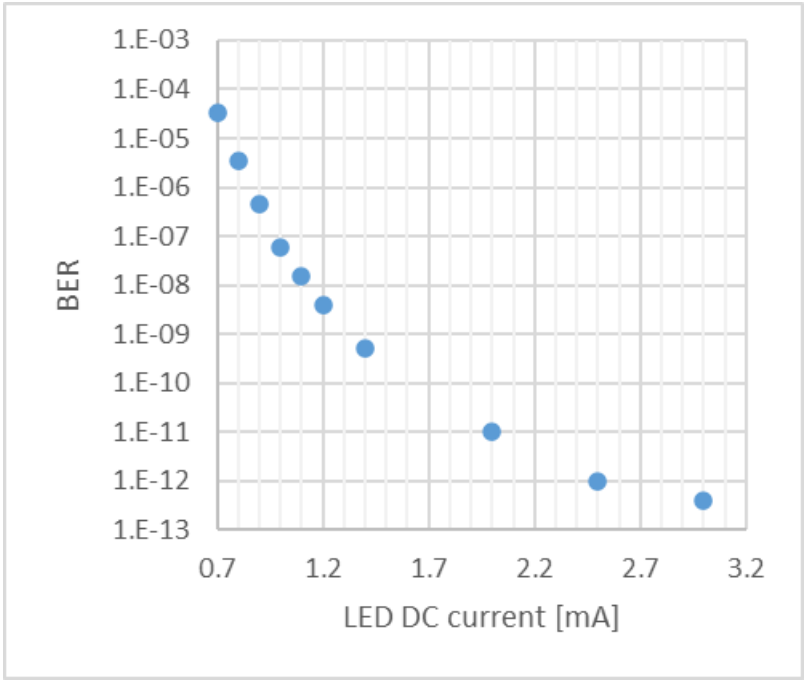


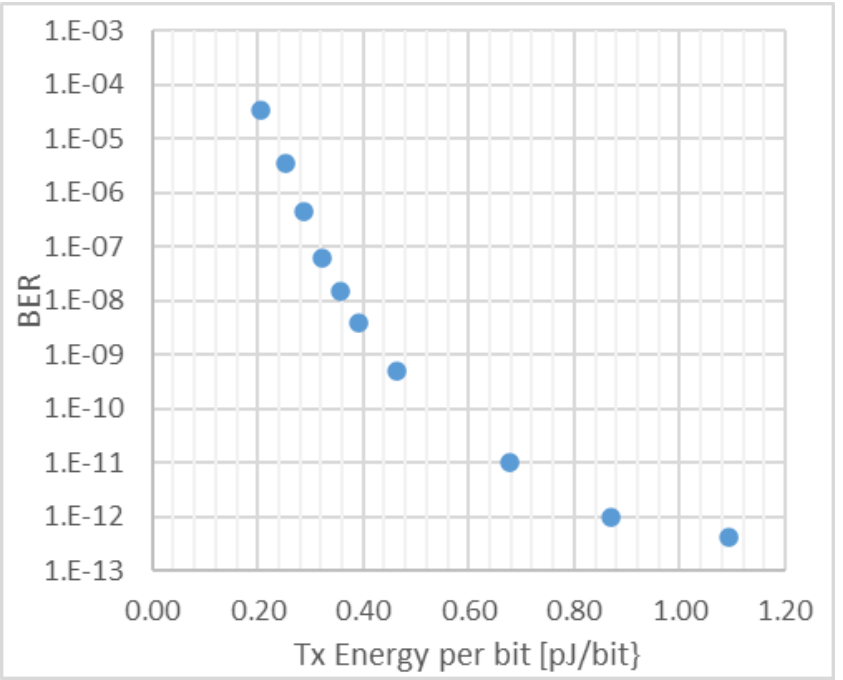
3mA LED current @BER 4E-13



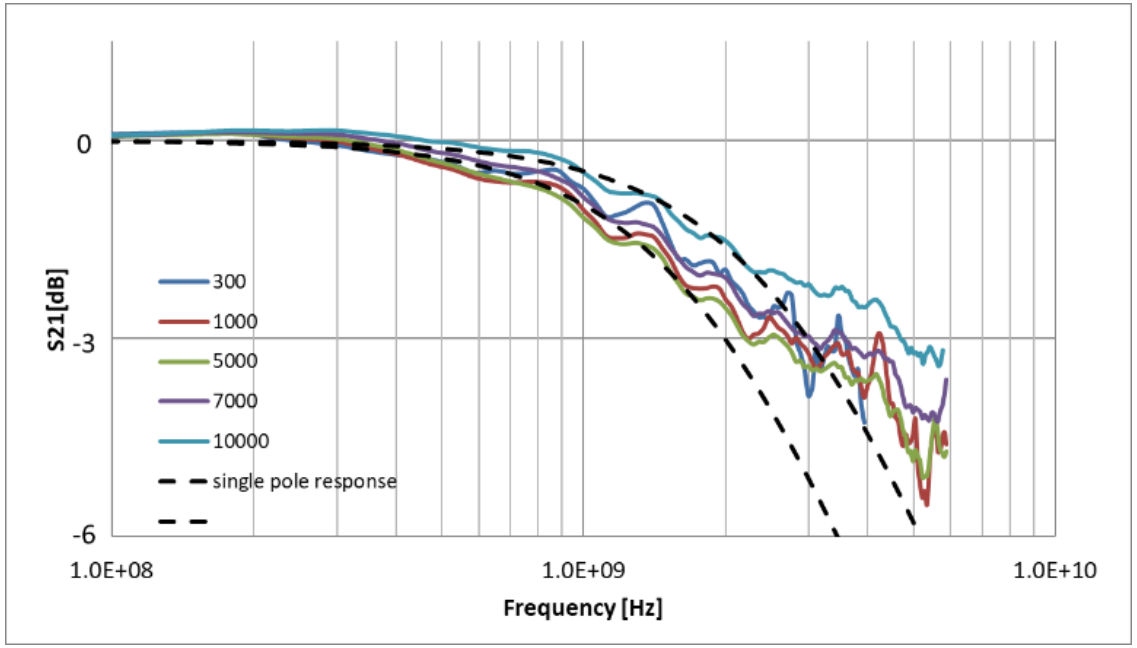
1.5mA LED current @BER 1E-9



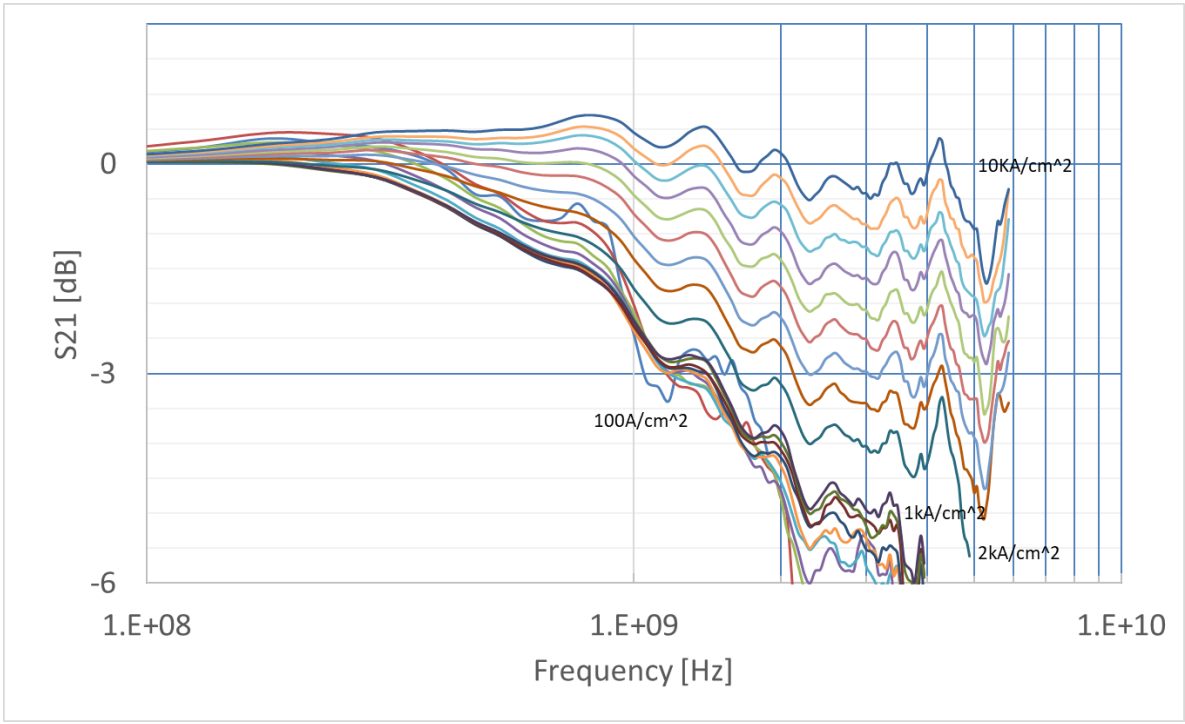




How fast are the LEDs?



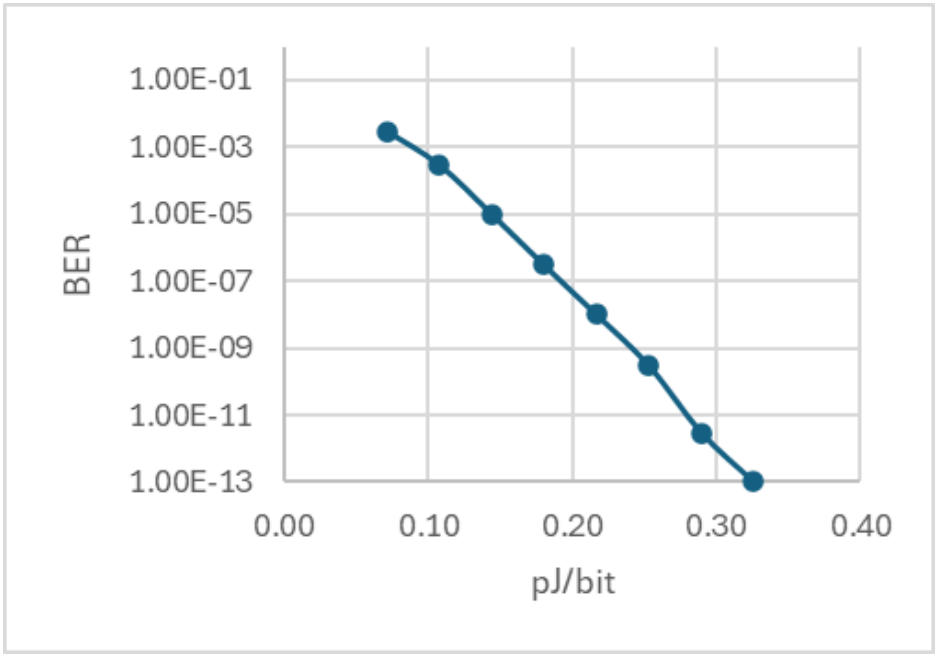
- Base high speed LED
- 3dB~ 5GHz
- But very slow roll-off



- Very high speed LED
- 1dB down at 6GHz
- Need better instruments!

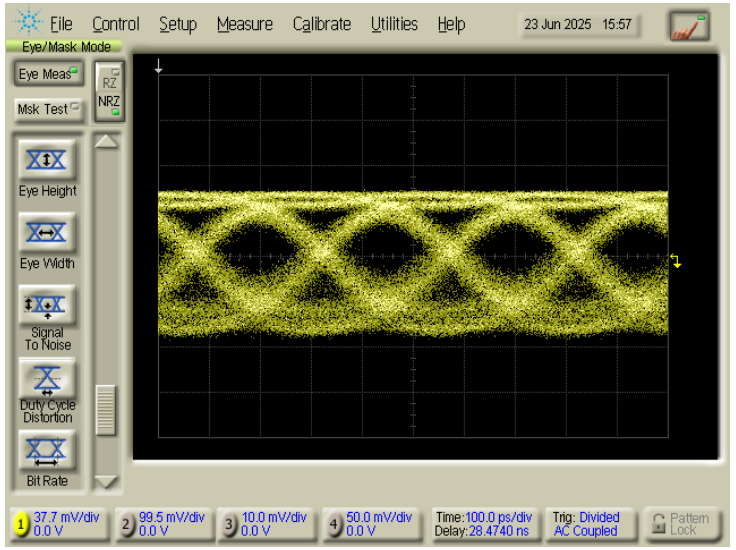
4Gb/s single link with TSMC detector samples

- Achieved record 0.2-0.3pJ/bit for Tx



4Gbps, P_in =3µW, I_LED= 250uA:

- BER ~3E-7 @ 0.20pJ/bit

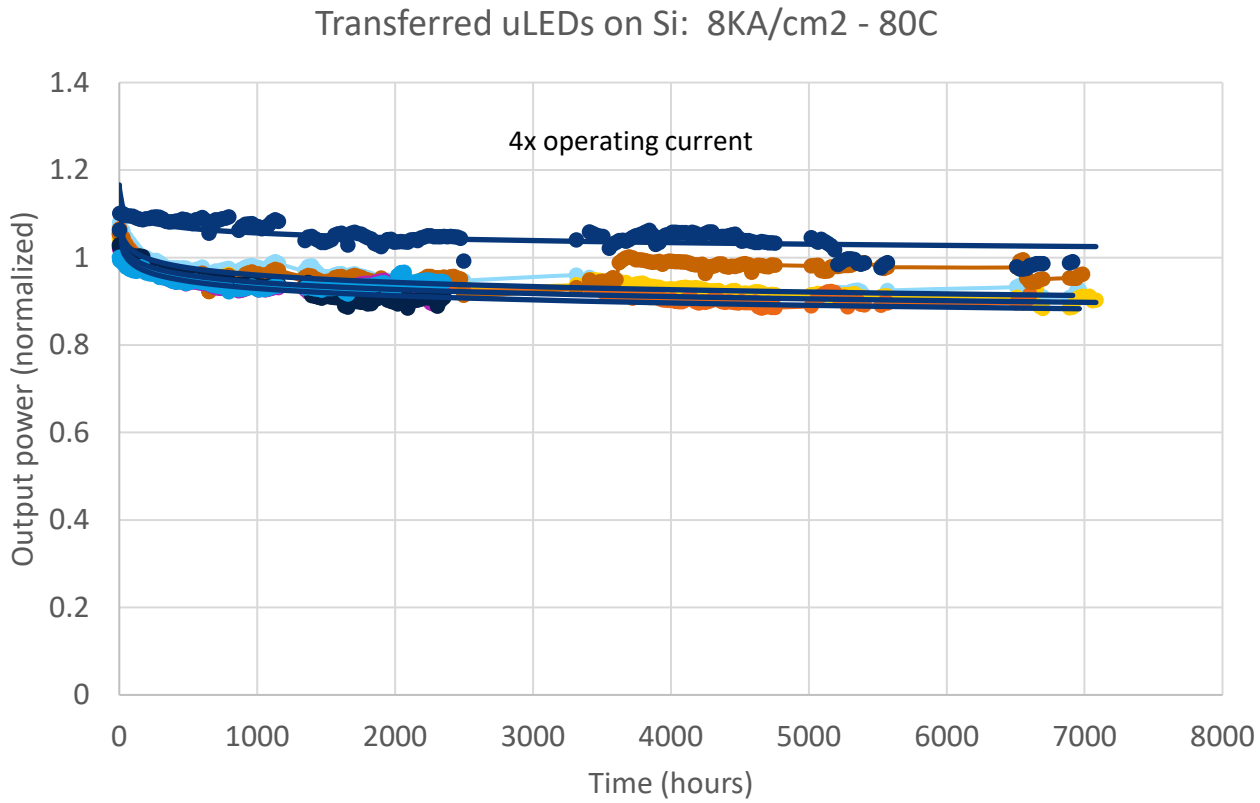


TSMC advanced detector link

* note, this is just Tx power. VCSEL, SiPh typically ~4pJ/bit. Our Rx ~0.35pJ/bit

Reliability

- Standard LEDs can’t really be driven at such high current densities
- Design modifications allow high reliability at high current



Avicena Patents

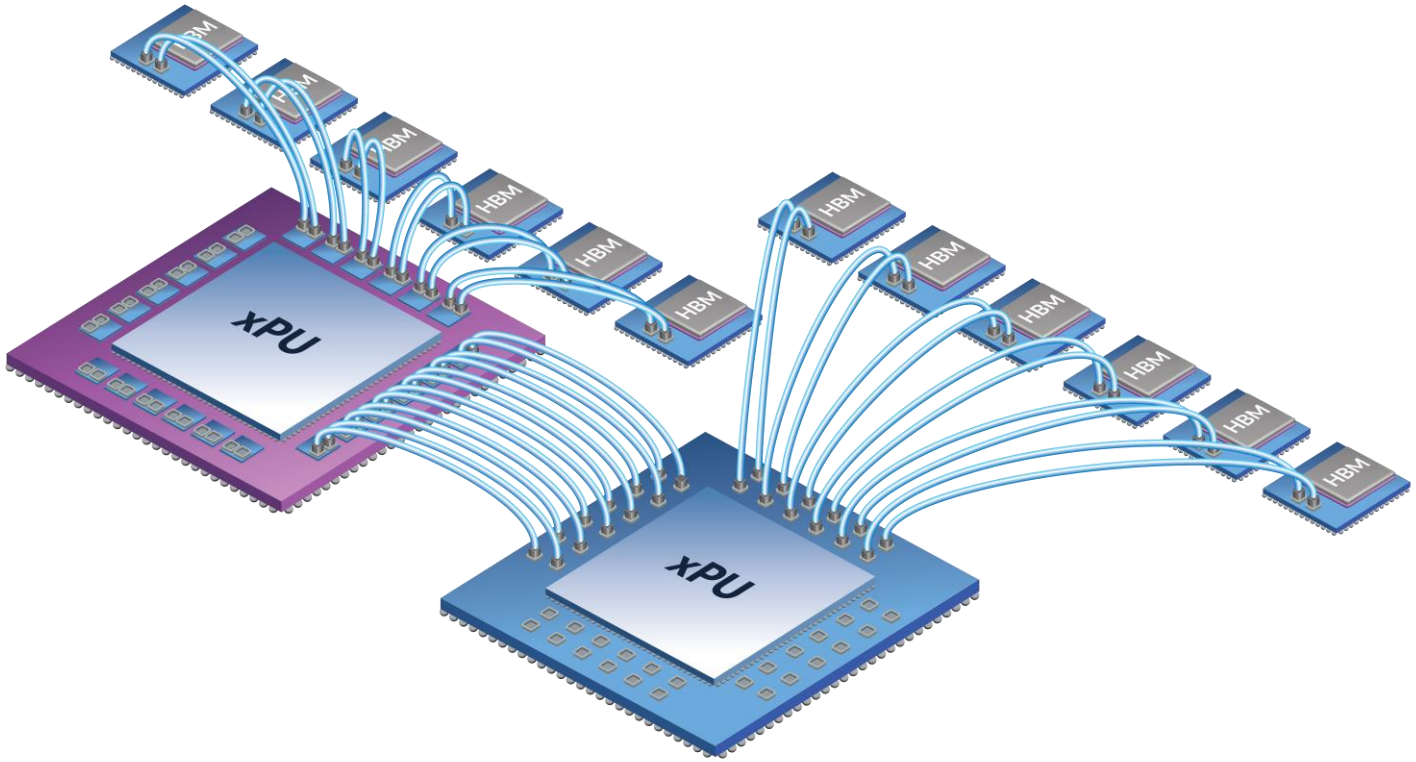
- Patent filings since in 2019
  - All directed to MicroLED optical interconnects
  - System level, component level, and more
    - It's not just the microLEDs, although it is that too!

- Over 40 issued patents
  - US and non-US
  - All directly applicable to MicroLED optical interconnects

- ~100 pending patent applications
  - In various stages of prosecution
  - Open continuations the norm
  - All directly applicable to MicroLED optical interconnects

Summary

- Large arrays of microLEDs can provide high bandwidth
- Demo with 4Gb/s array, but much higher per lane speeds are possible
- Can achieve very low pJ/bit
- Potential applications in
  - AOCs
  - CPO scale-up in AI
  - Memory interfaces with HBM



Thank You!

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